

FIG. 1

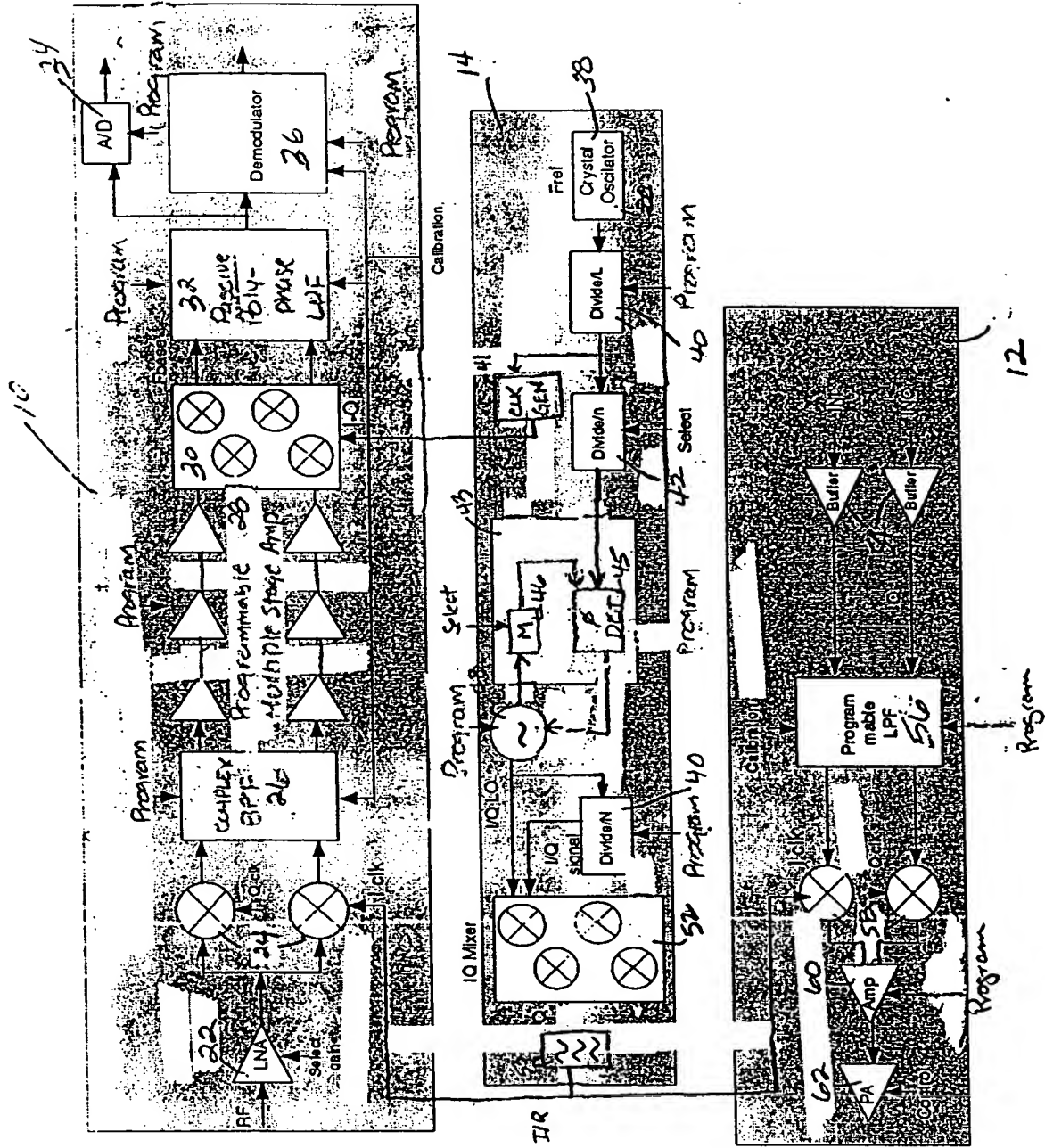


FIG. 2

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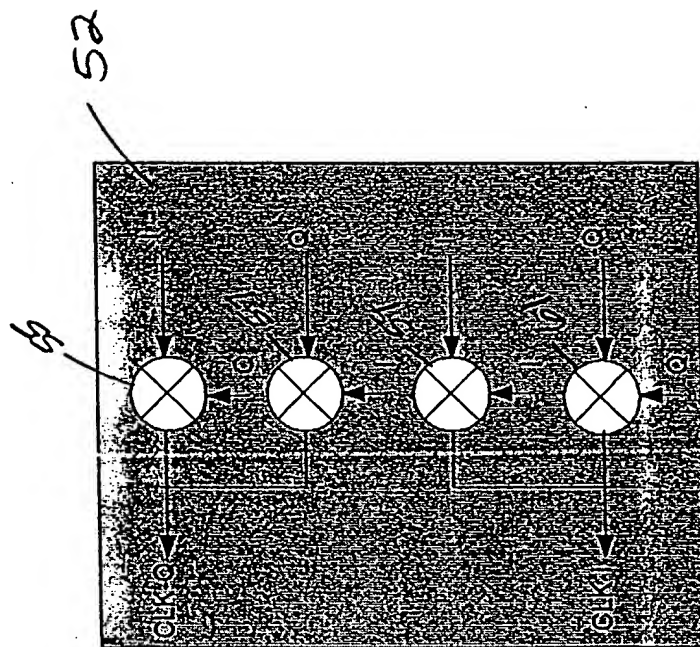


FIG. 3

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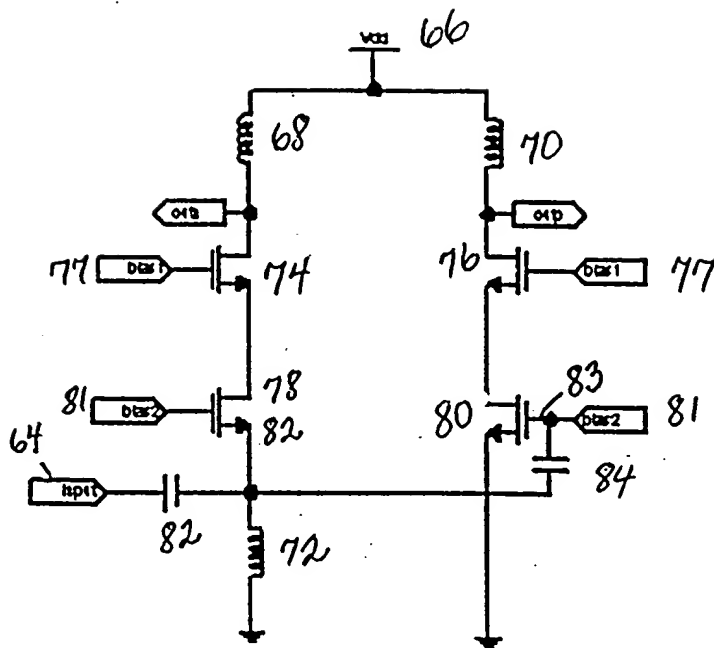


FIG. 4

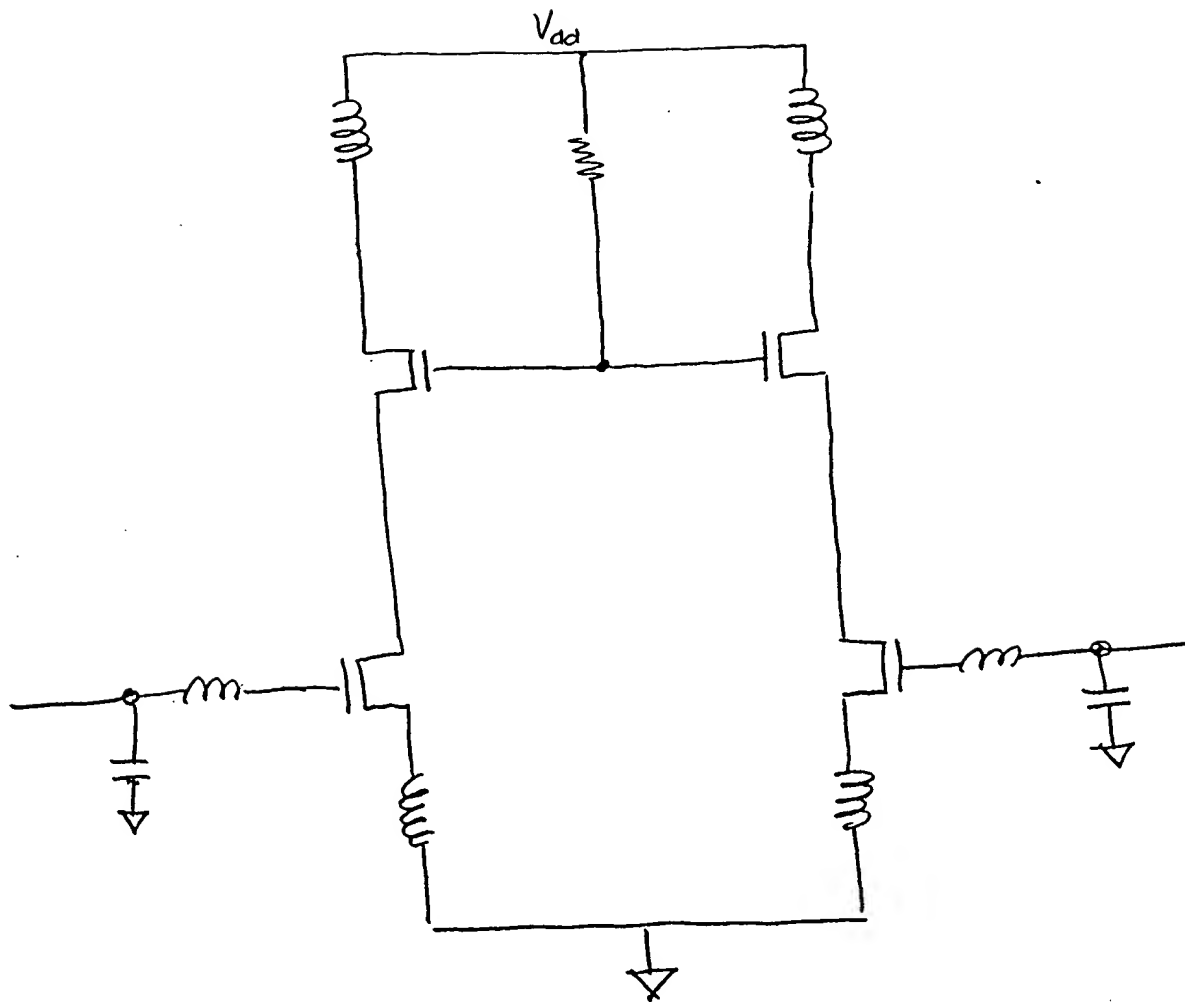


FIG. 4(a)

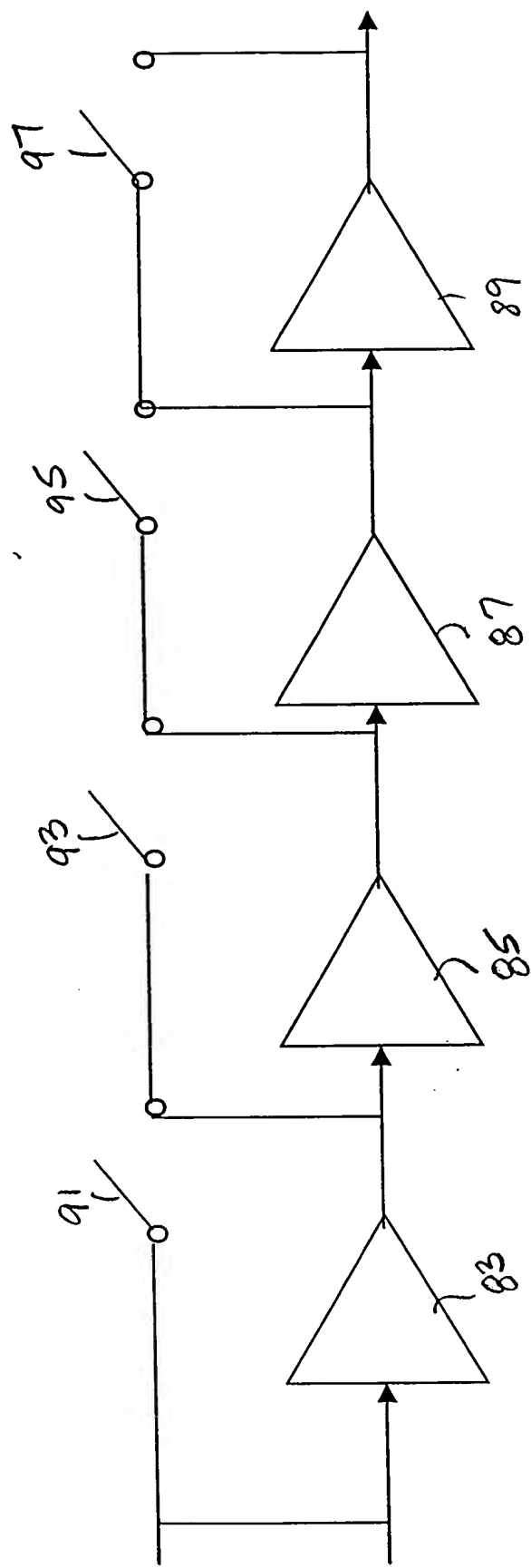


FIG. 5

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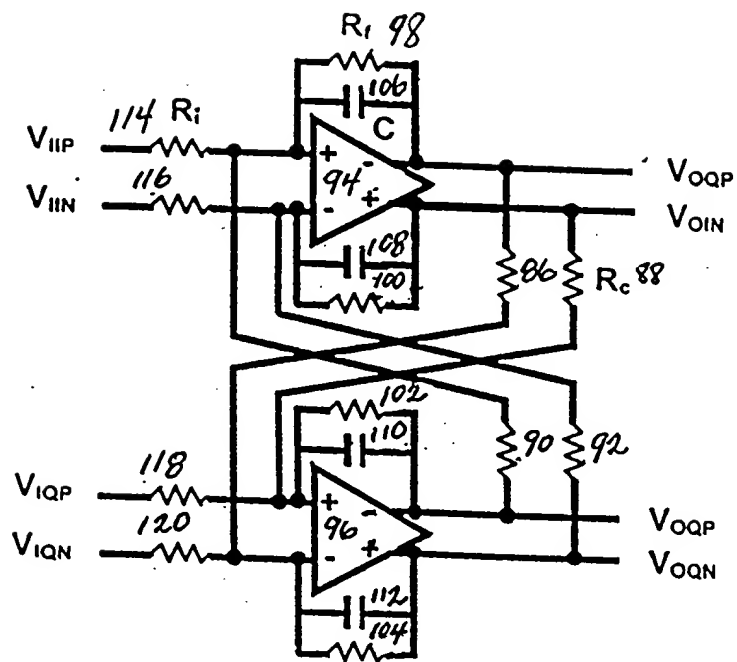


FIG. 6

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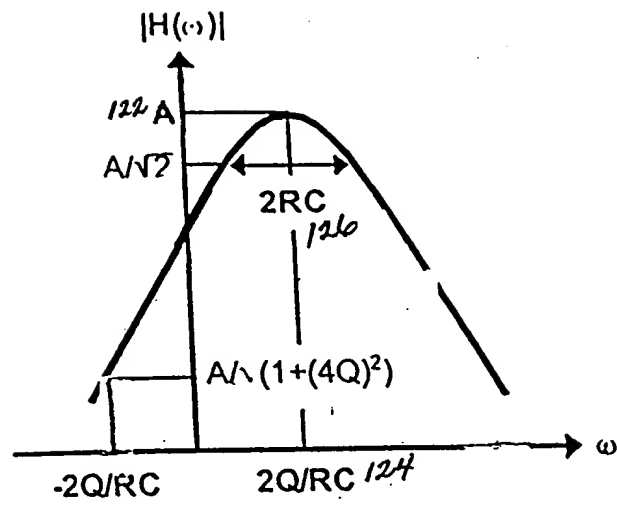


FIG. 7



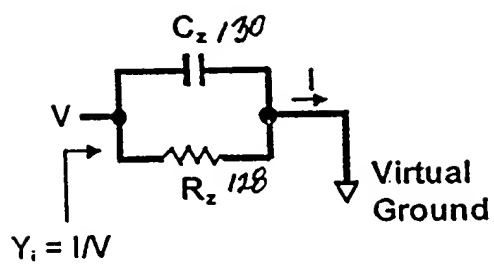


FIG. 8

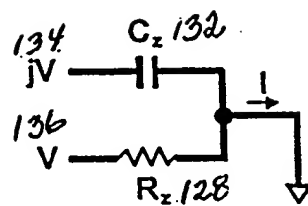


FIG. 9

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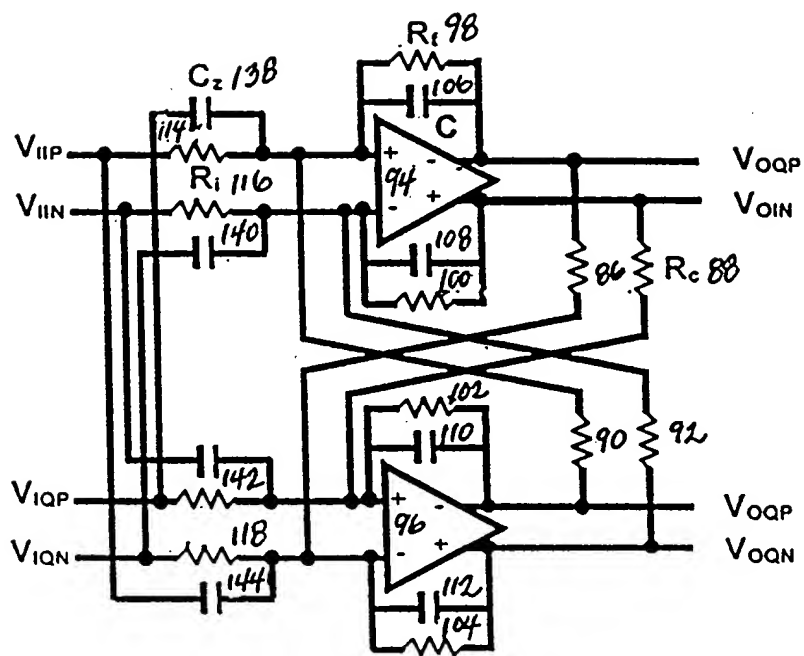


FIG. 10

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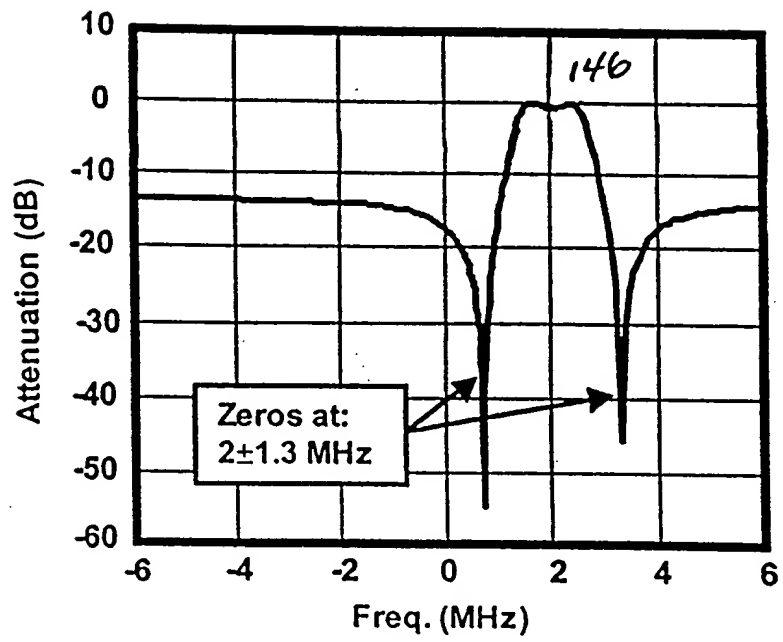


FIG. 11

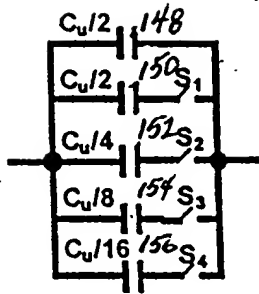


FIG. 12(a)

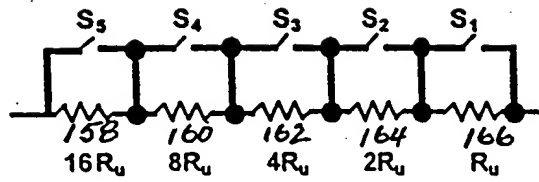


FIG. 12(b)

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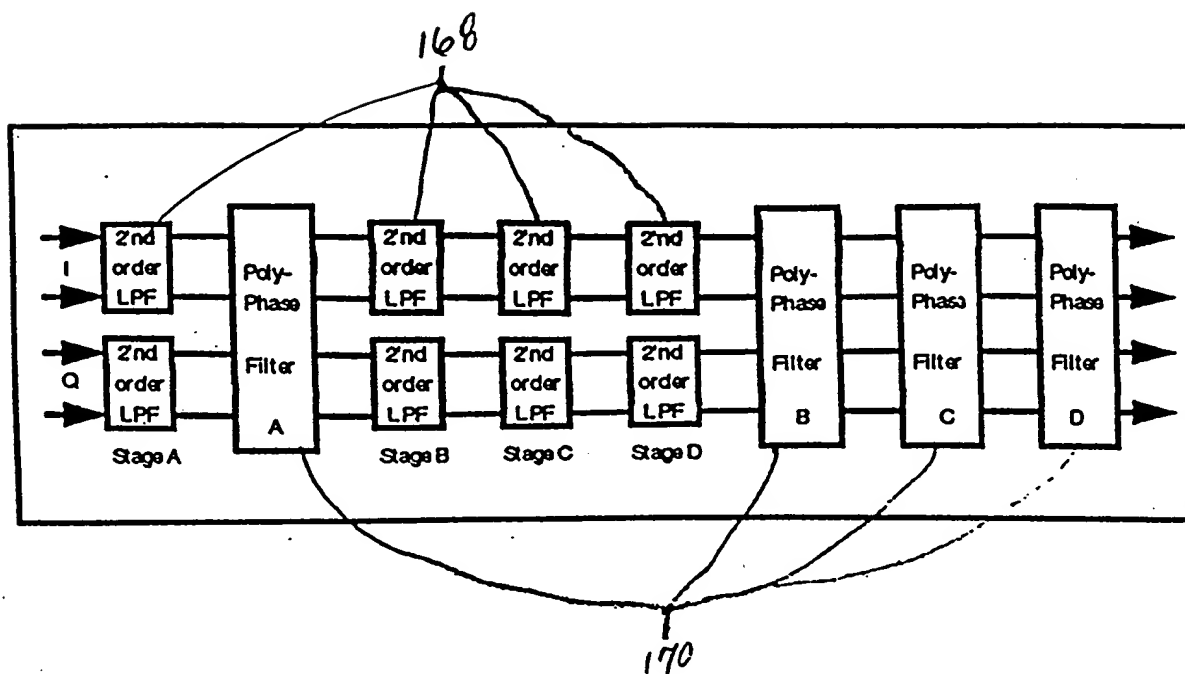


FIG. 13

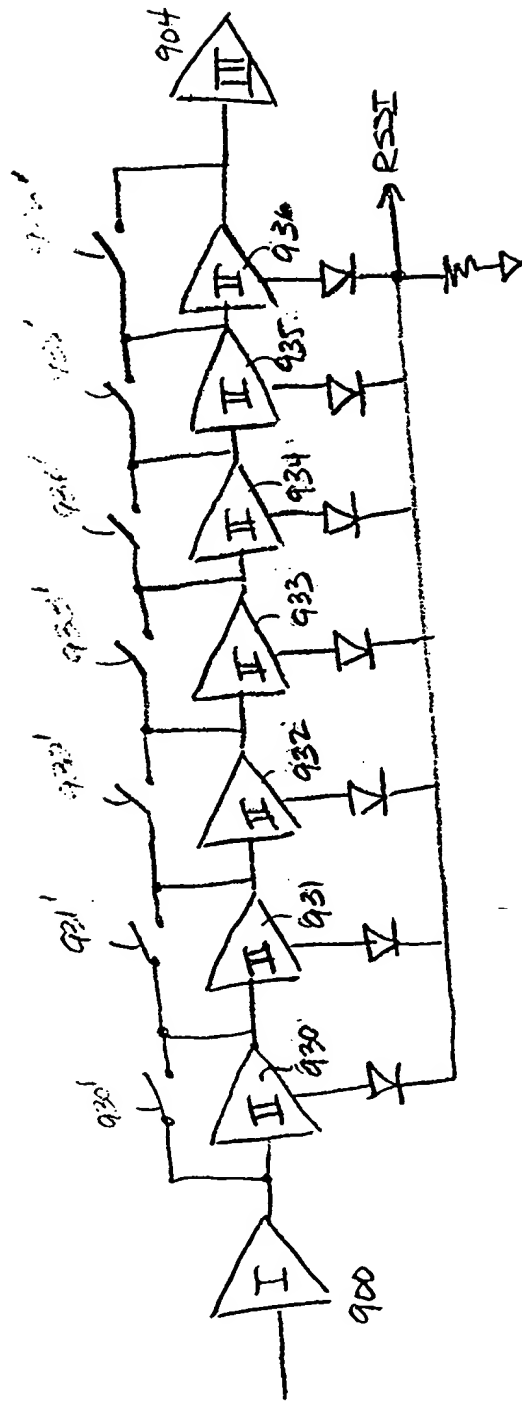


FIG. 14

09698437.102700

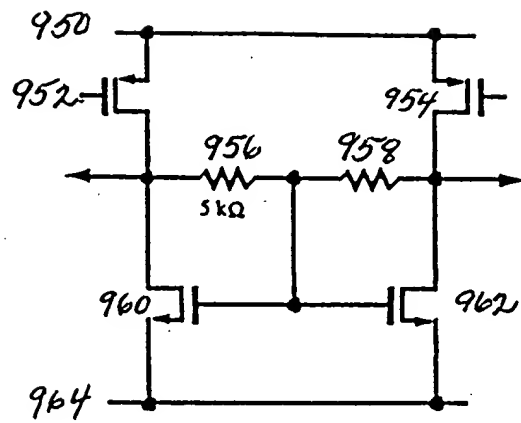


FIG. 15

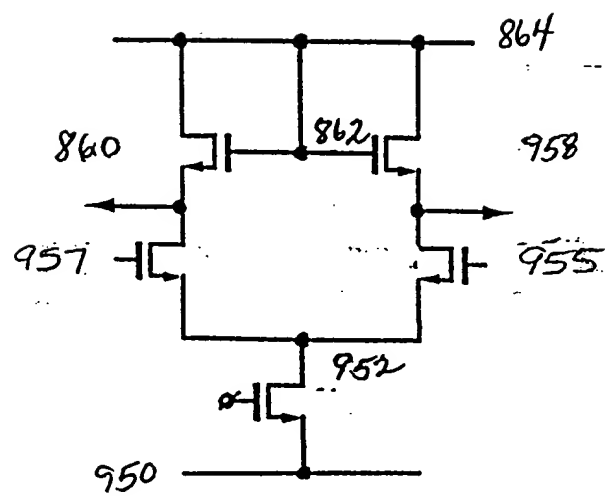


FIG. 1b(a)



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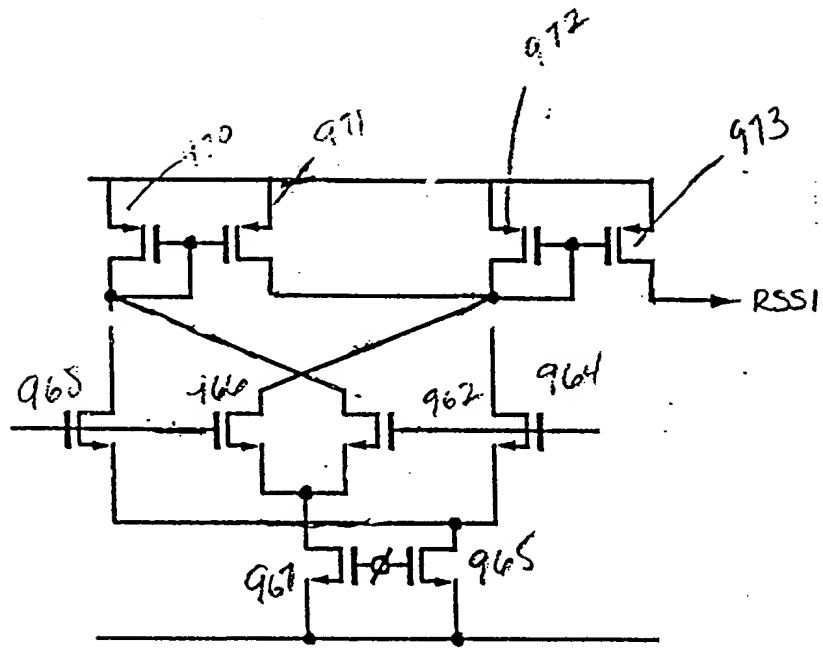


FIG. 16(b)

FIG. 17(a)

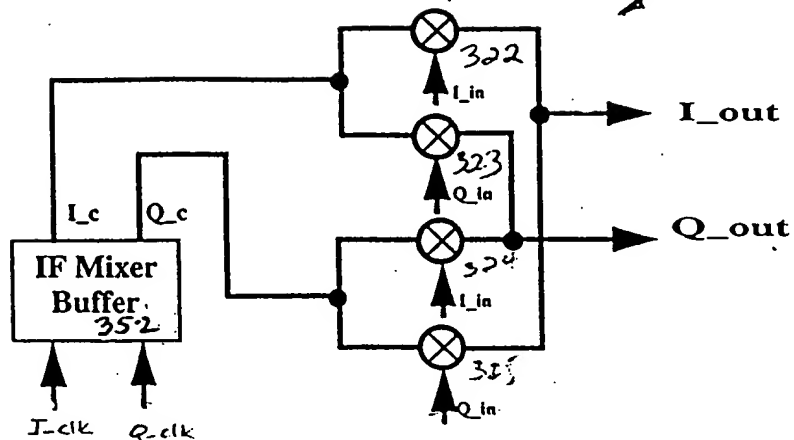


FIG. 17(b)

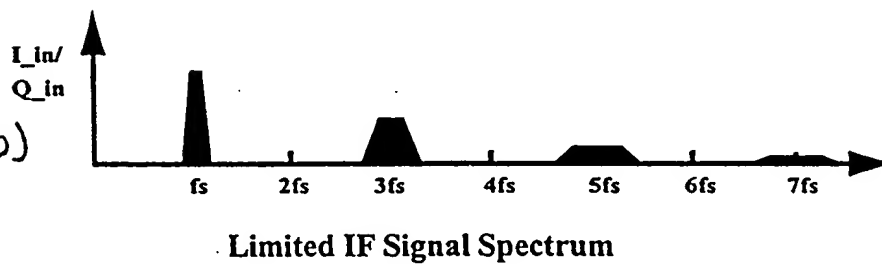


FIG. 17(c)

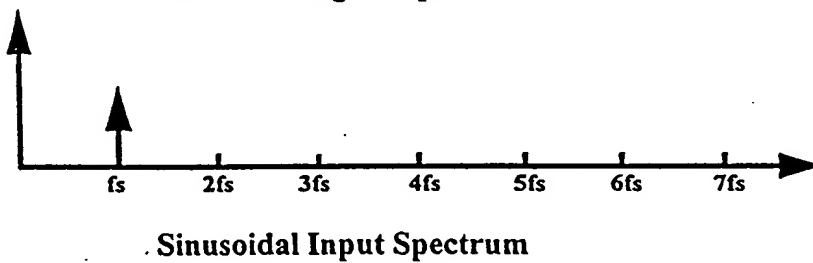
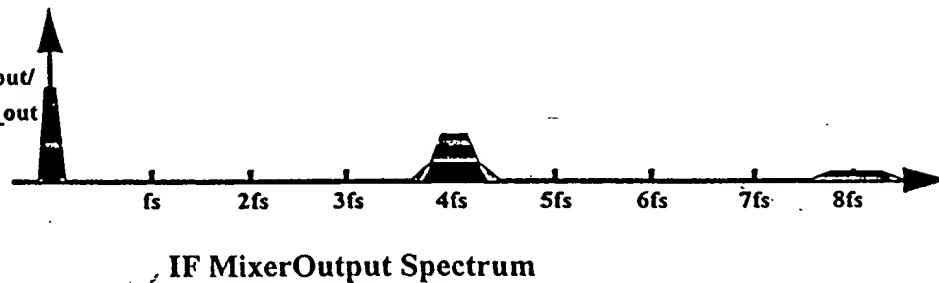


FIG. 17(d)



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FIG. 18

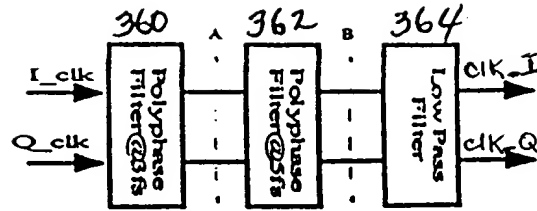


FIG. 19(a)

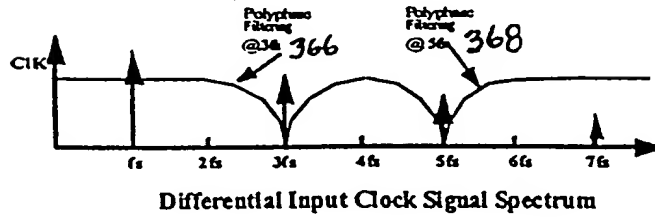


FIG. 19(b)

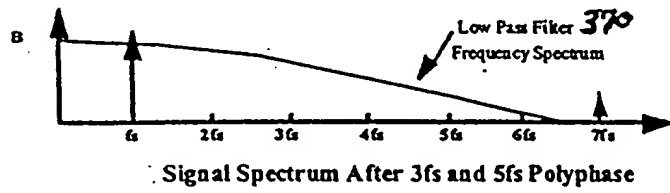
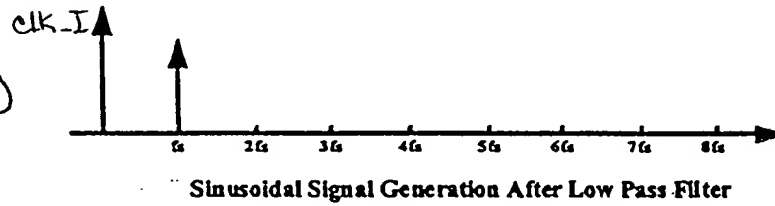


FIG. 19(c)



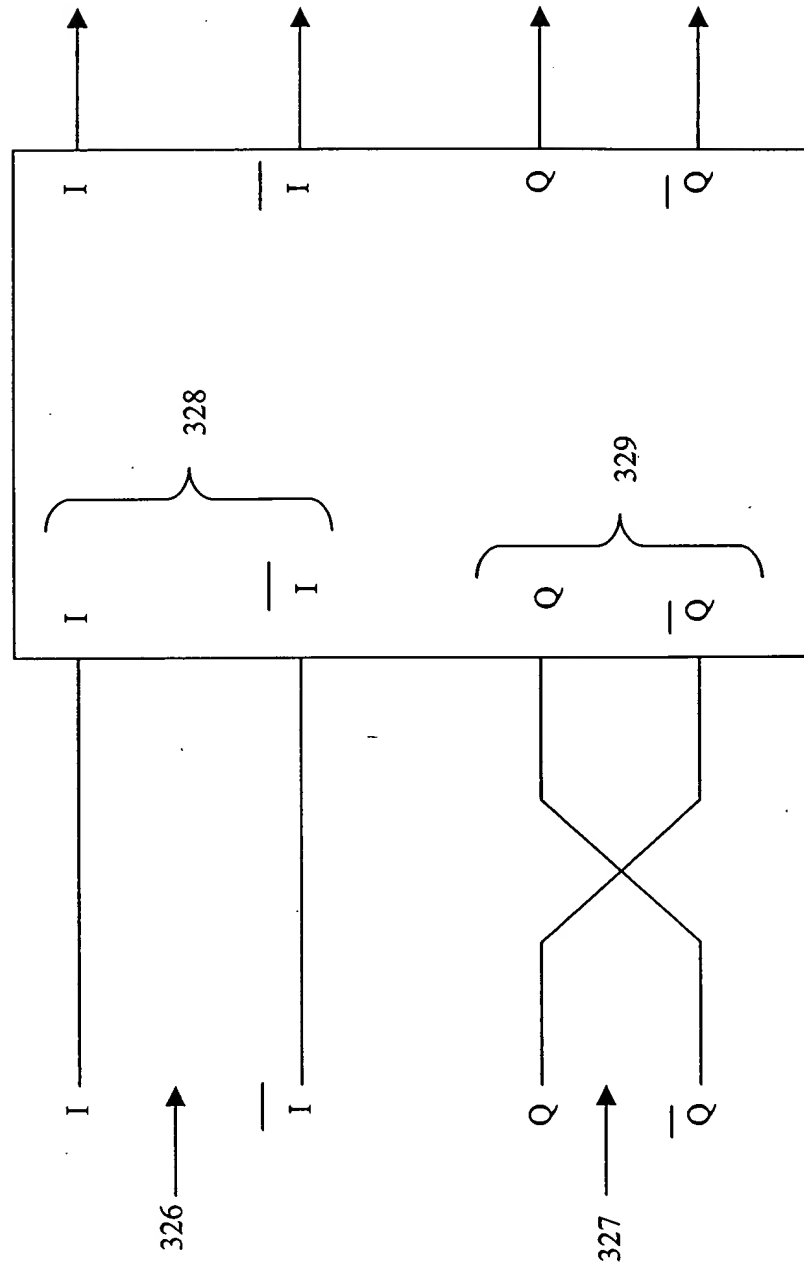


FIG. 19d

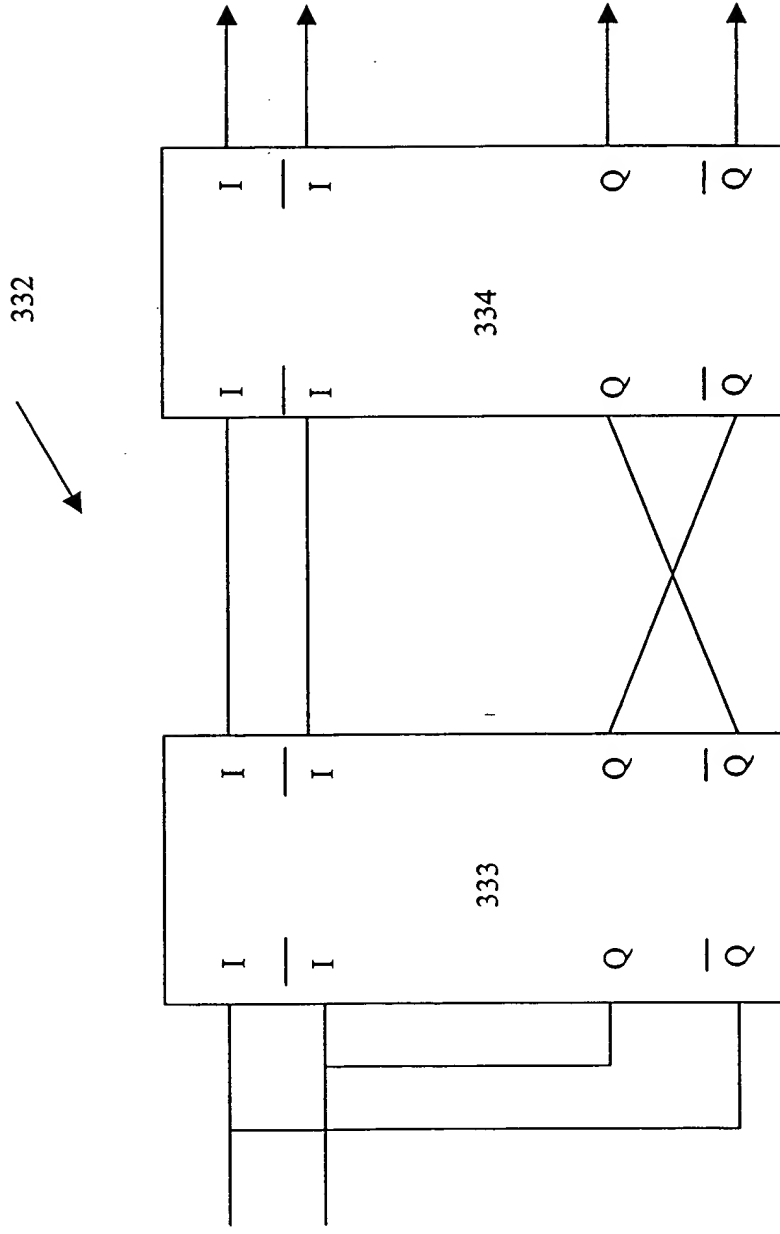


FIG. 19e

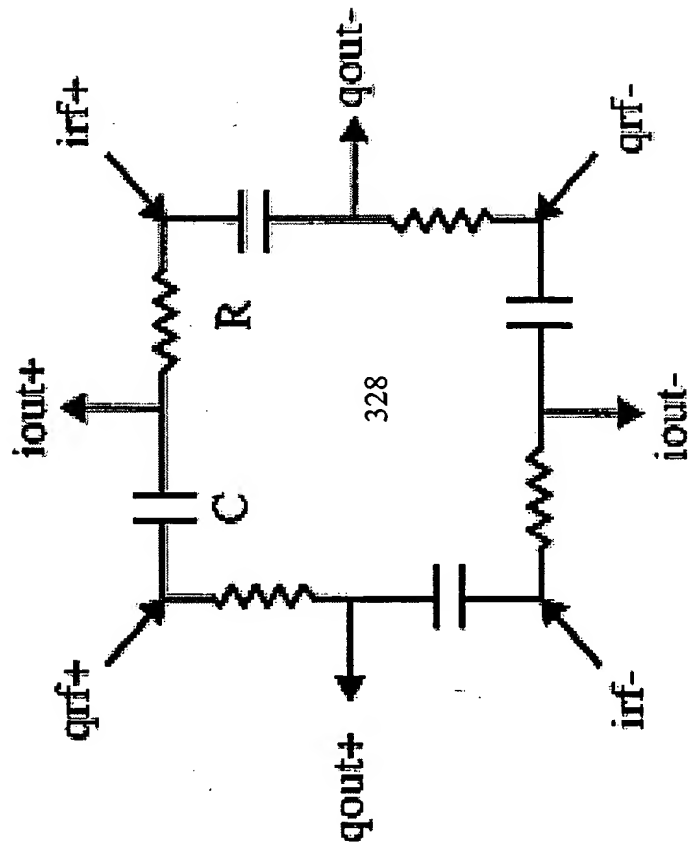
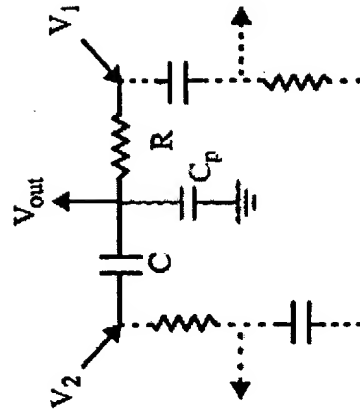


FIG. 19f



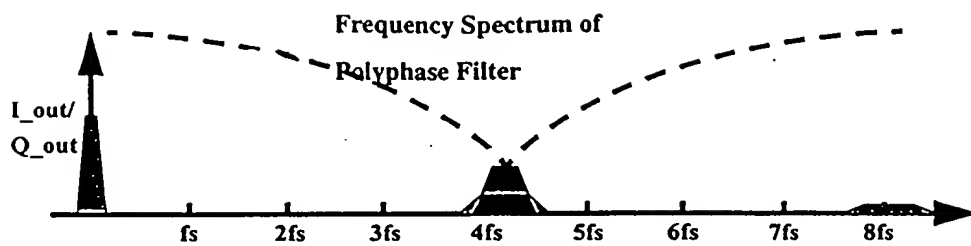
$$\omega_p = \frac{1}{R(C_p + C)}$$

$$\omega_o = \frac{1}{RC}$$

$$V_{out} = \frac{V_1}{R(C_p + C)s + 1} + \frac{V_2RCs}{R(C_p + C)s + 1}$$

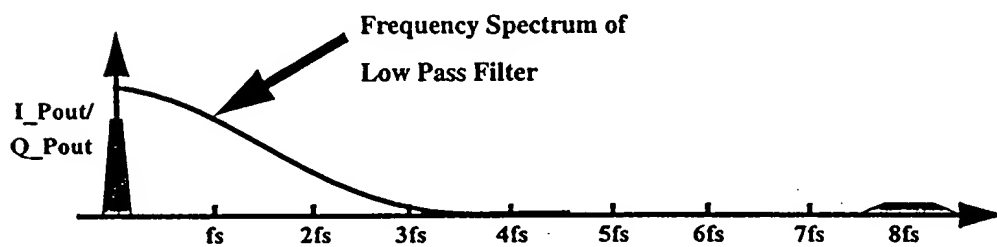


FIG. 19g



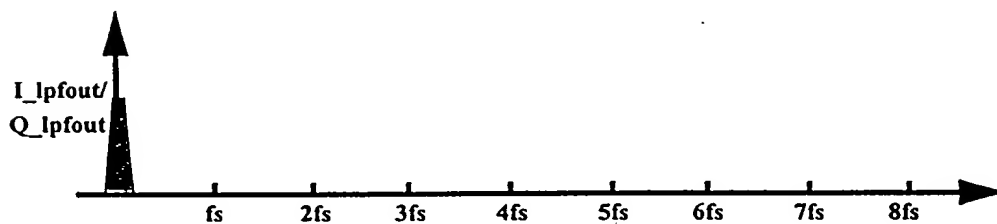
Signal Spectrum at Polyphase Input

FIG. 20(a)



Signal Spectrum at Polyphase Output

FIG. 20(b)



Signal Spectrum at Low Pass Filter Output

FIG. 20(c)



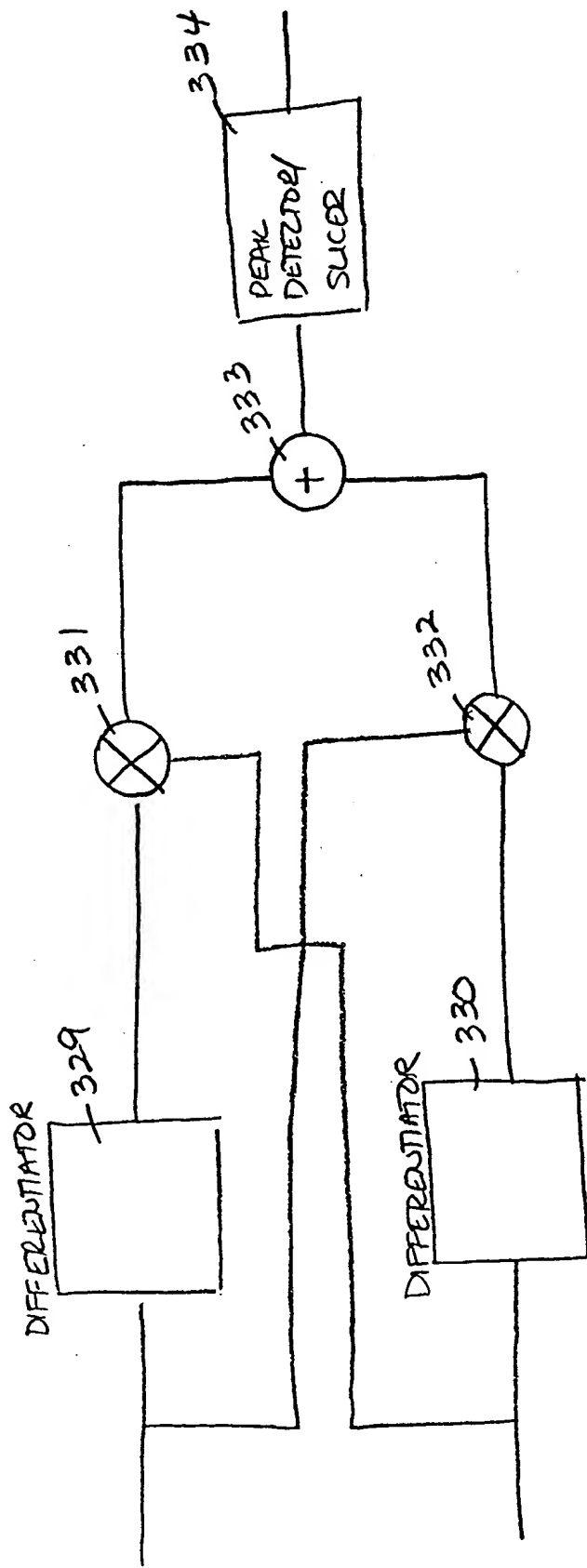


FIG. 21

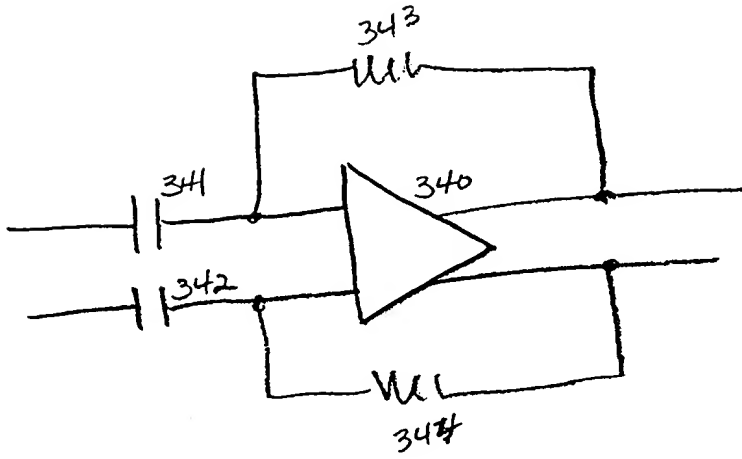


FIGURE 22

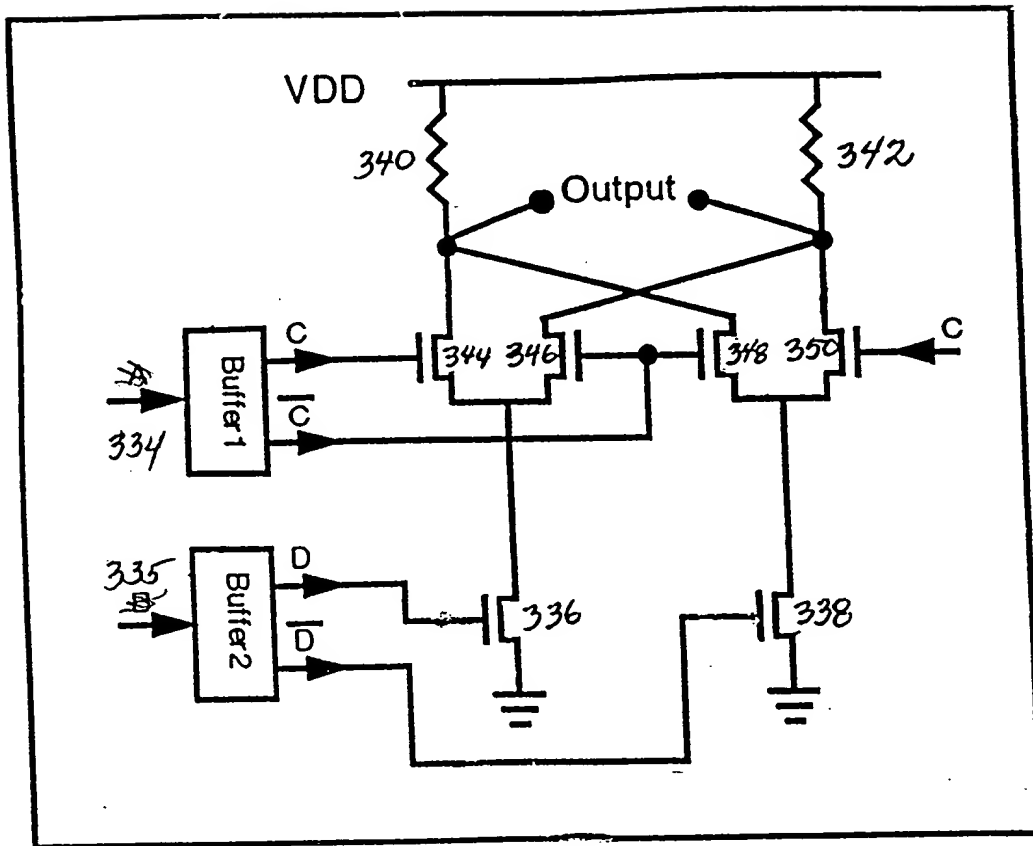


FIG. 23

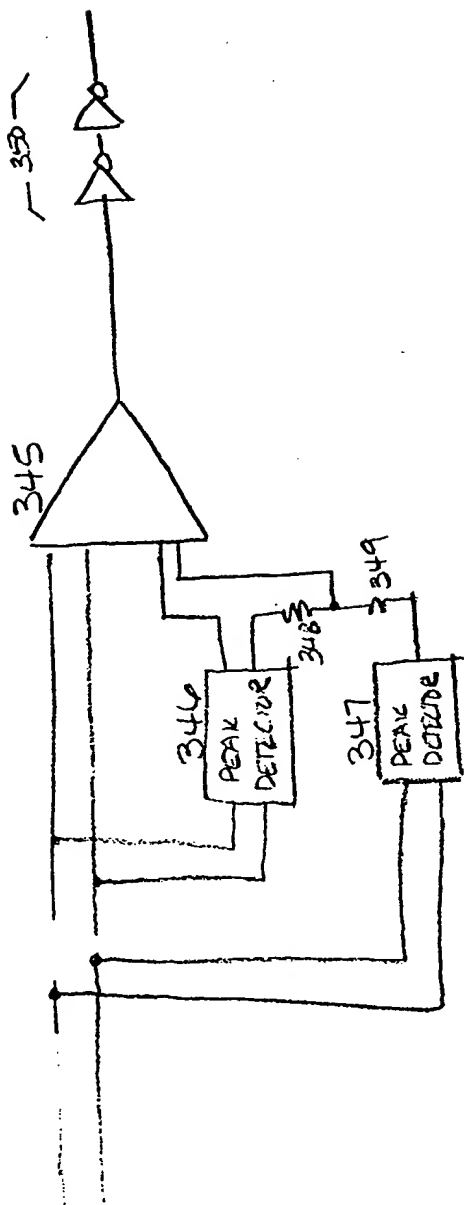


FIGURE 24



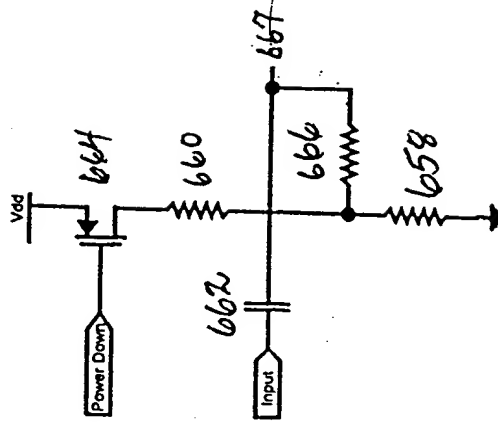


FIG. 26(b)

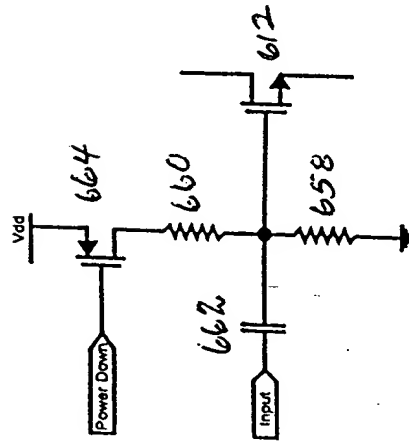


FIG. 26(a)

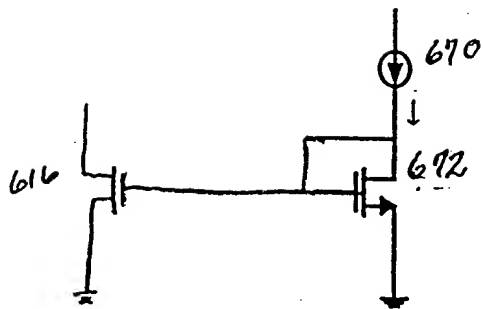


FIG. 27

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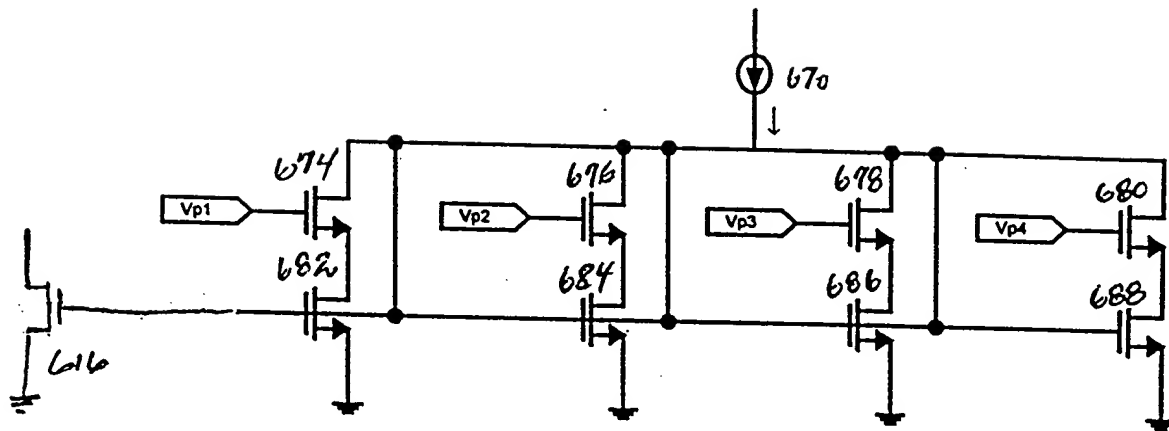


FIG. 28



Hand-drawn schematic diagram of a 700 MHz receiver circuit. The circuit includes a 6016 preamplifier, a 690 resistor, a 692 resistor, a 694 resistor, a 696 resistor, a 698 resistor, a 700 resistor, a 702 resistor, a 704 resistor, a 706 resistor, a 708 resistor, a 710 resistor, a 712 resistor, a 714 resistor, a 716 resistor, a 718 resistor, and a 720 resistor. The circuit is powered by a 500V source and a 50 ohm load. Annotations include "Coupling" and "Connection of the two nodes effectively matches to 50 ohms".

FIG. 29

002207-102700

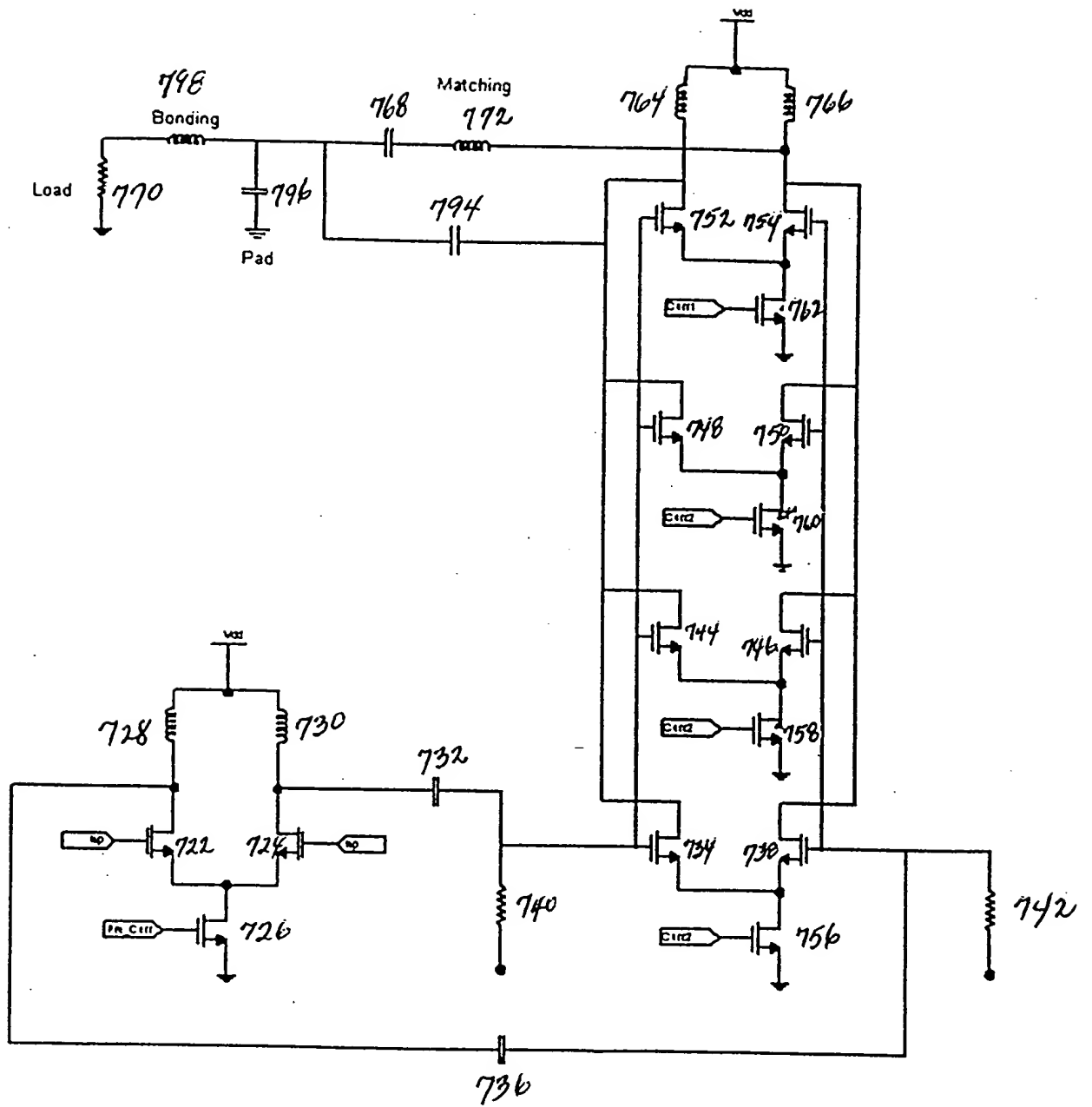


FIG. 30A

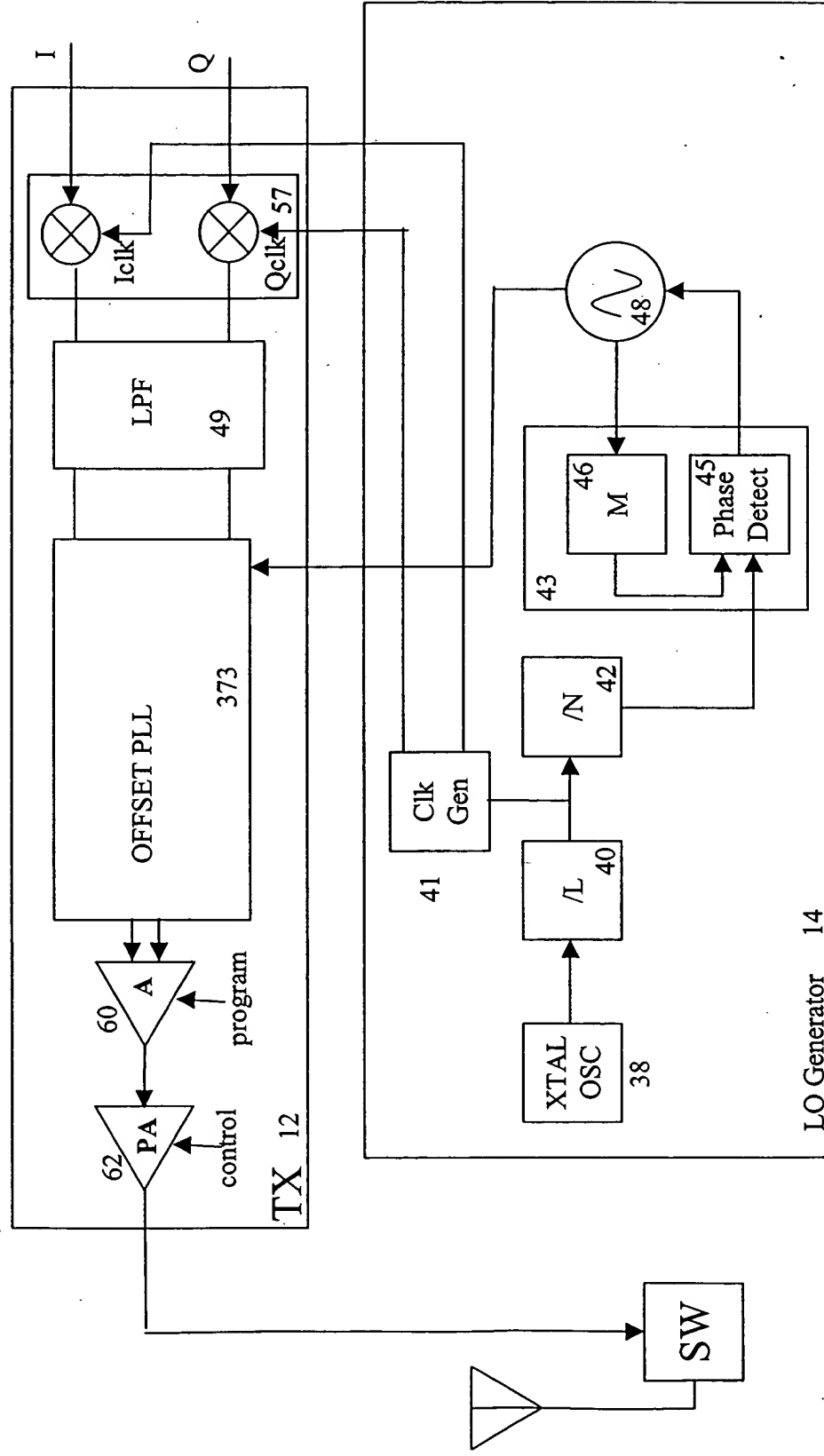


FIG. 30b

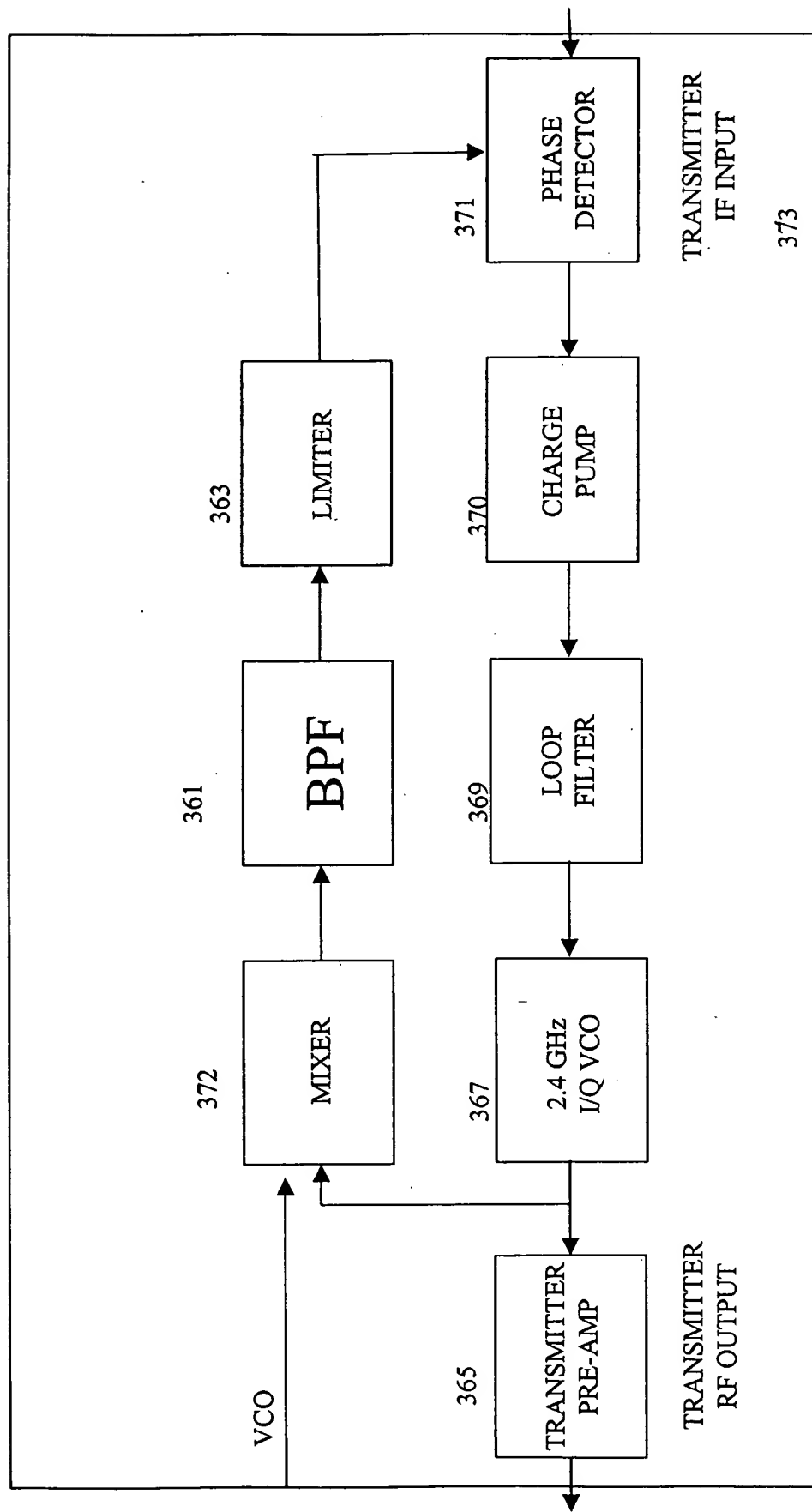


FIG. 30c

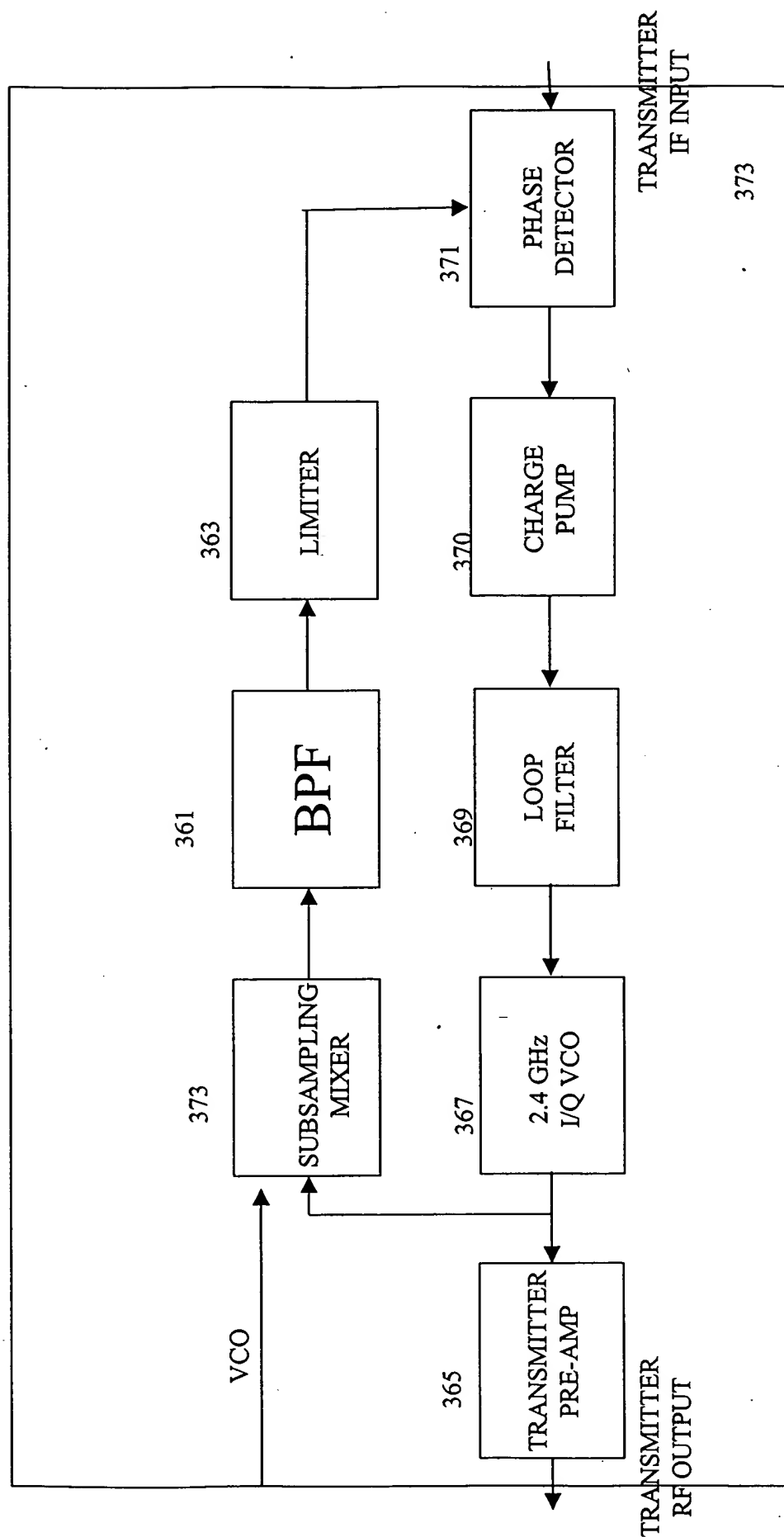


FIG. 30d

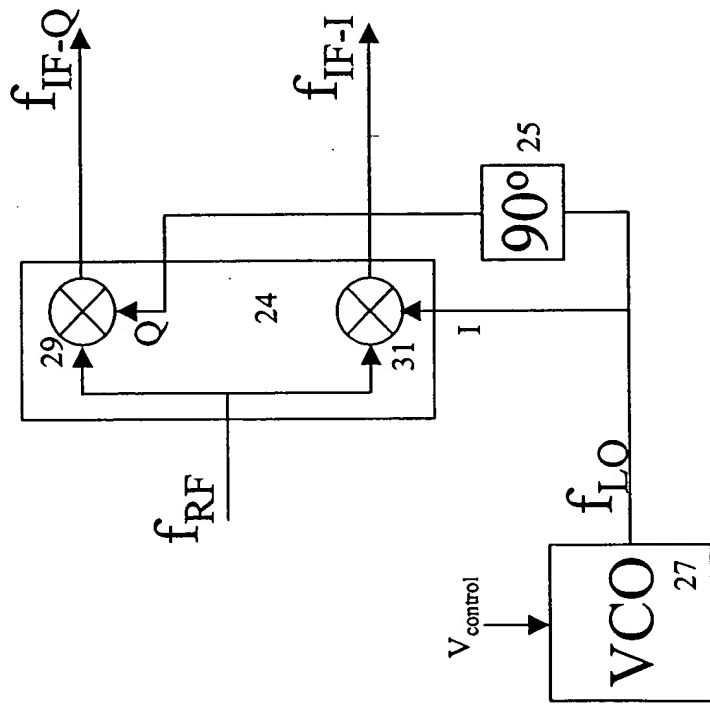


FIG. 30e

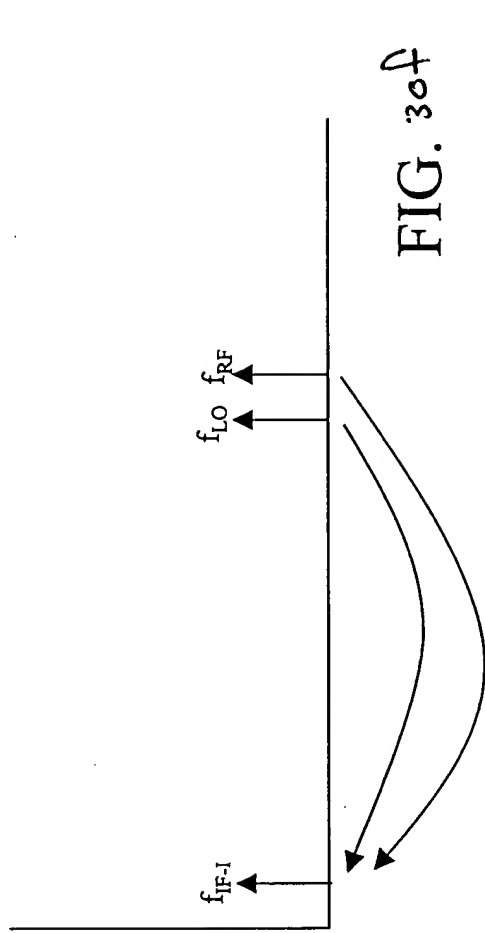


FIG. 30f

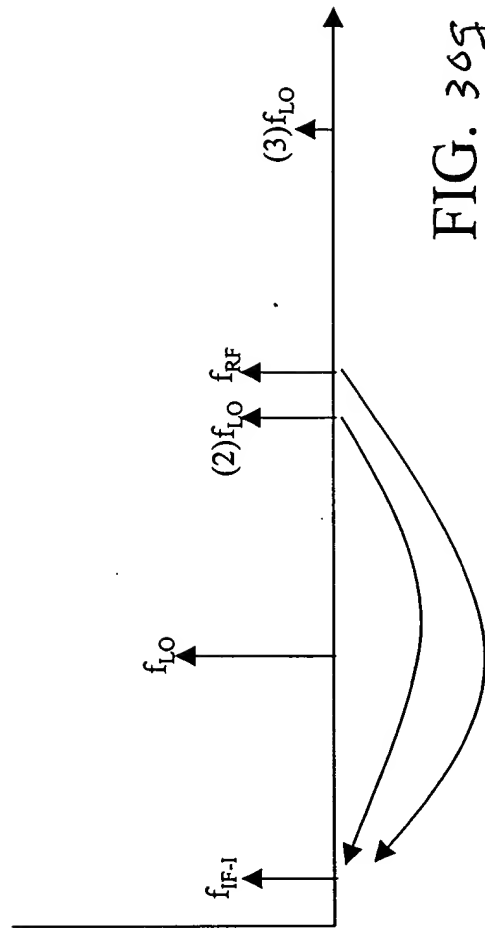


FIG. 30g

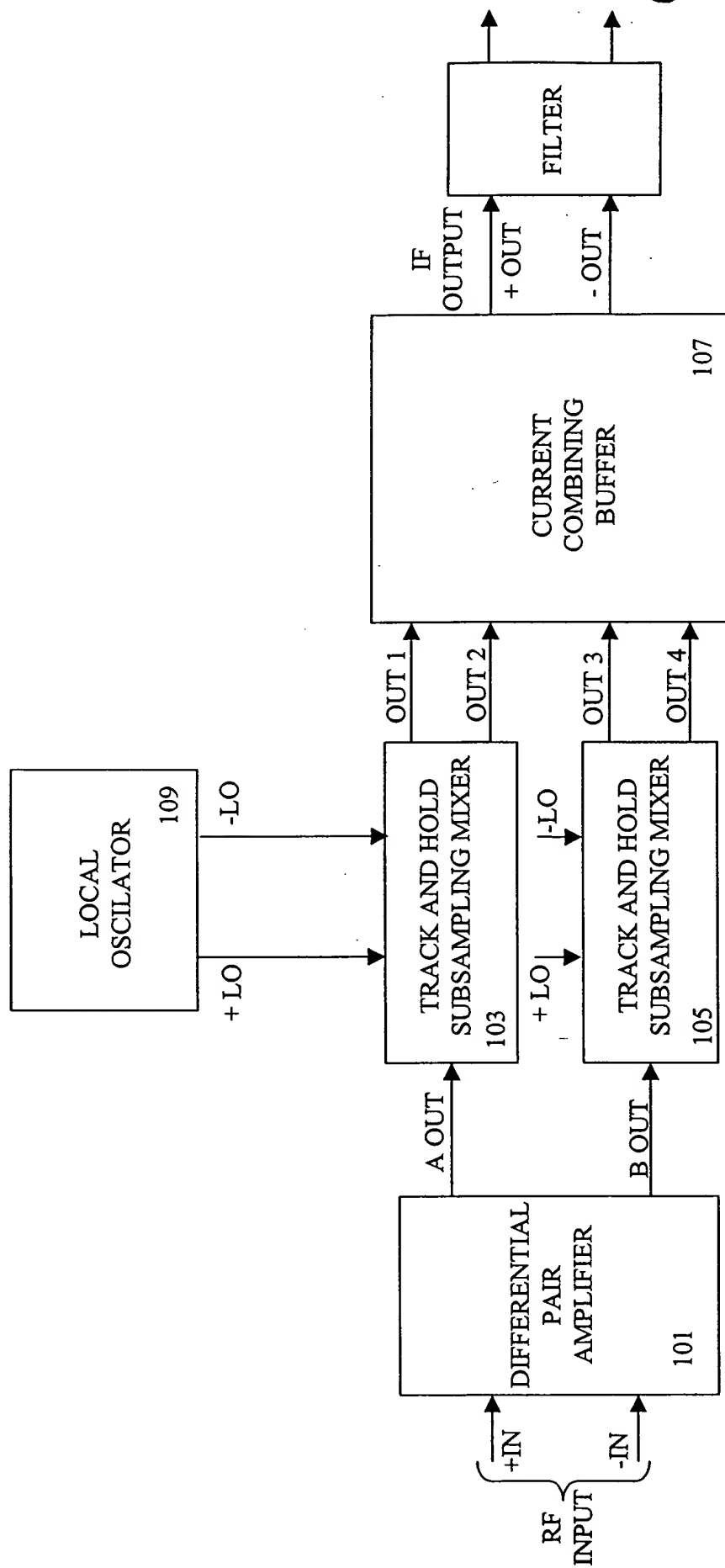


FIG. 30a

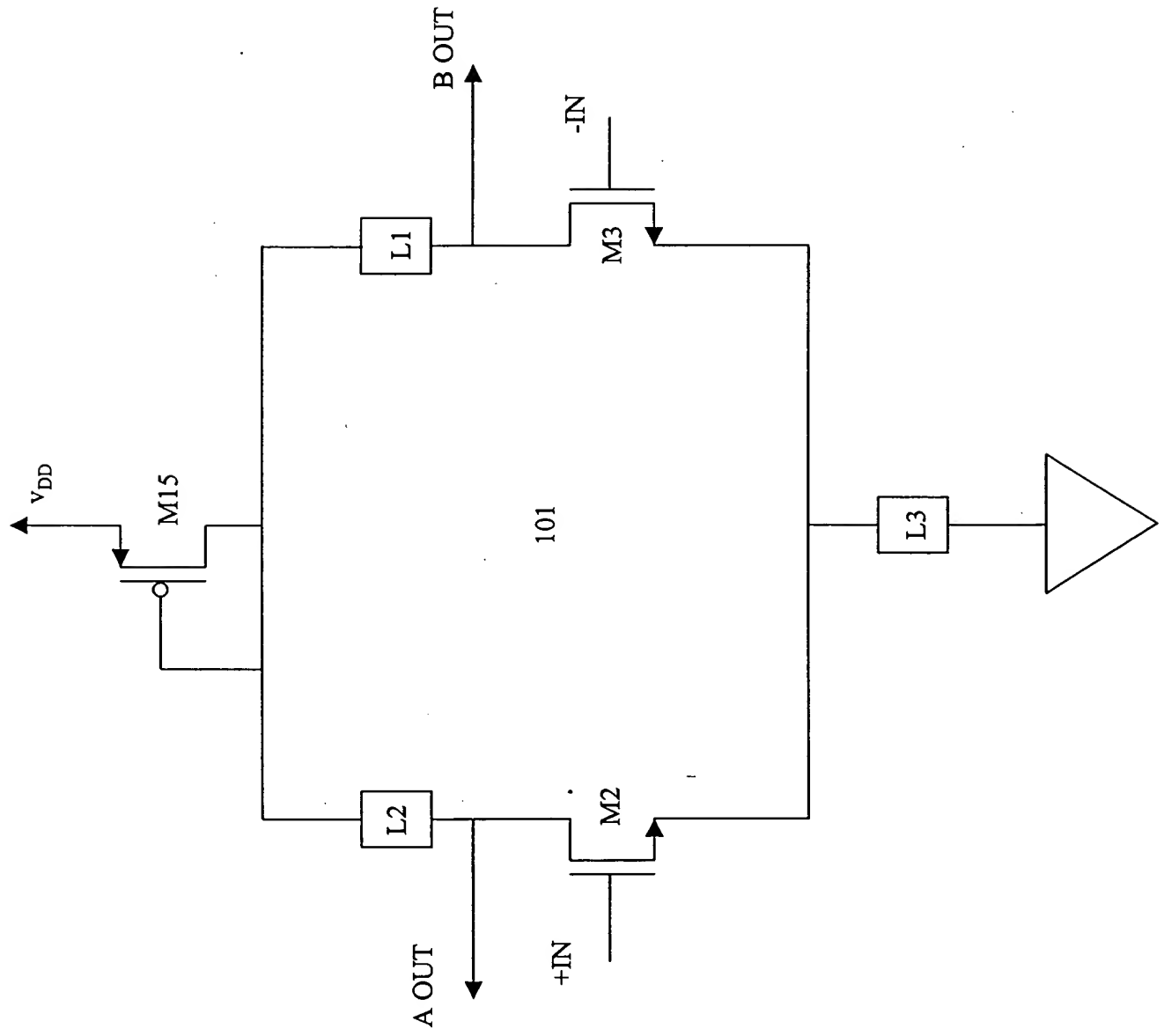
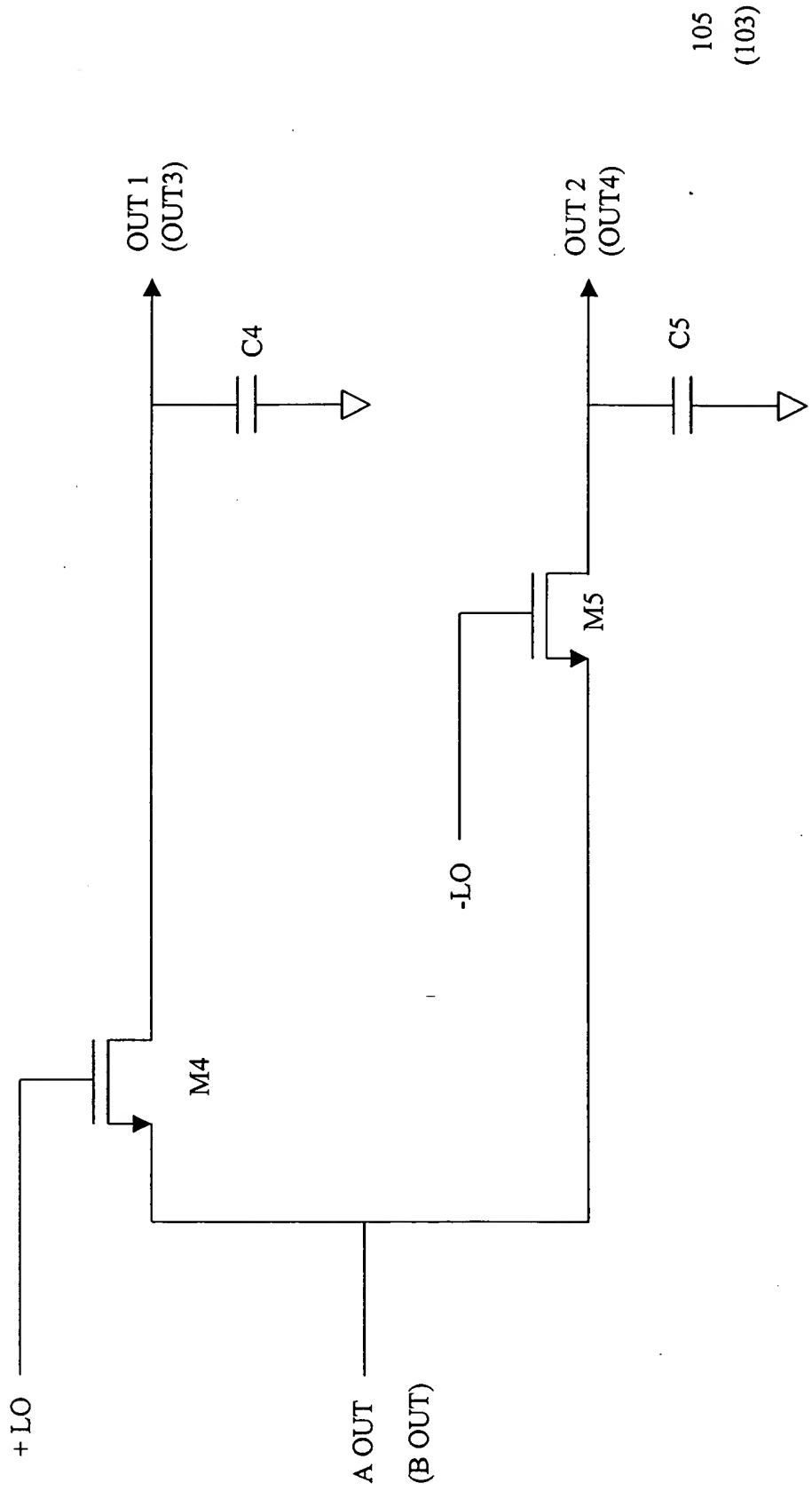


FIG. 30λ





105  
(103)

FIG. 30j

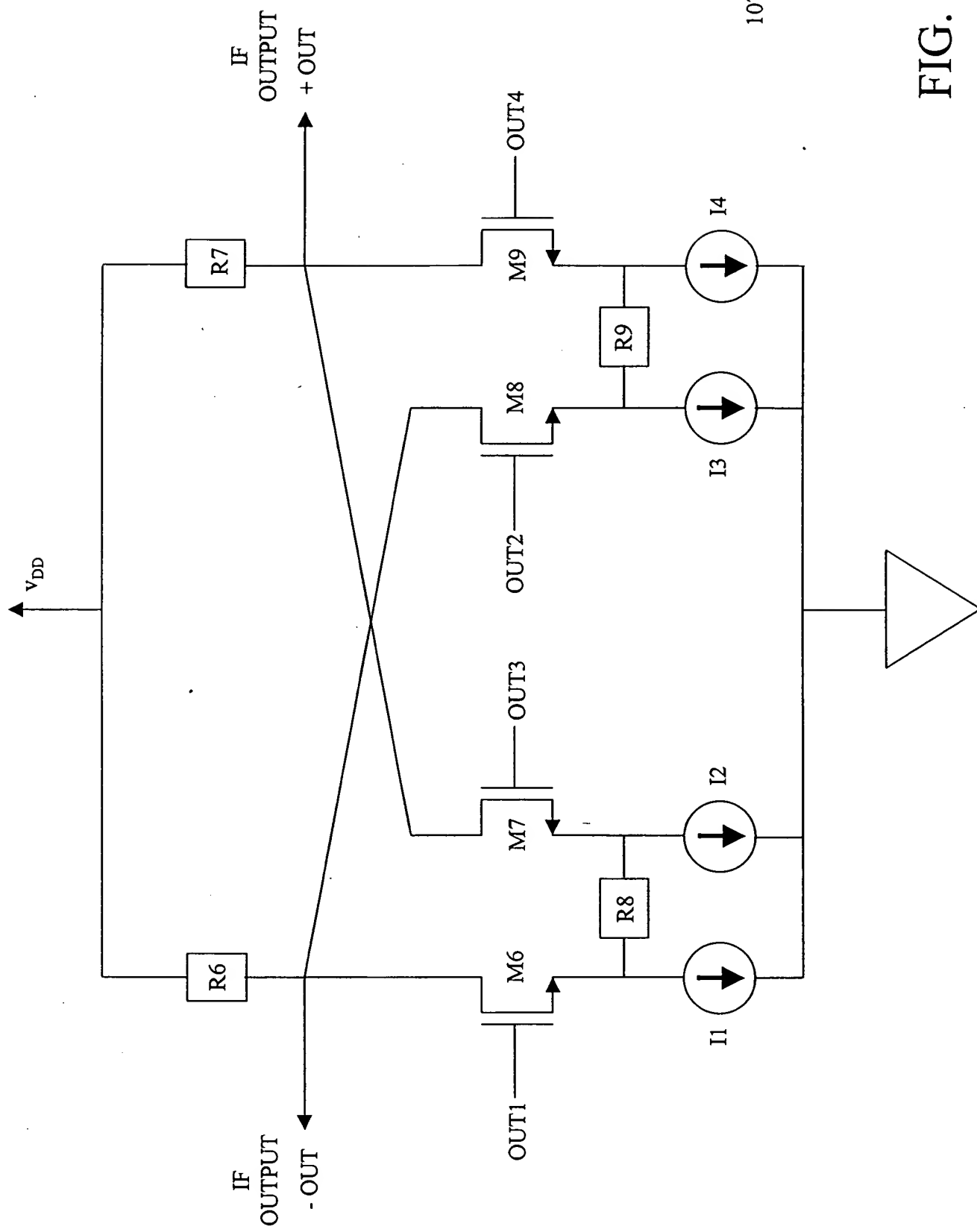
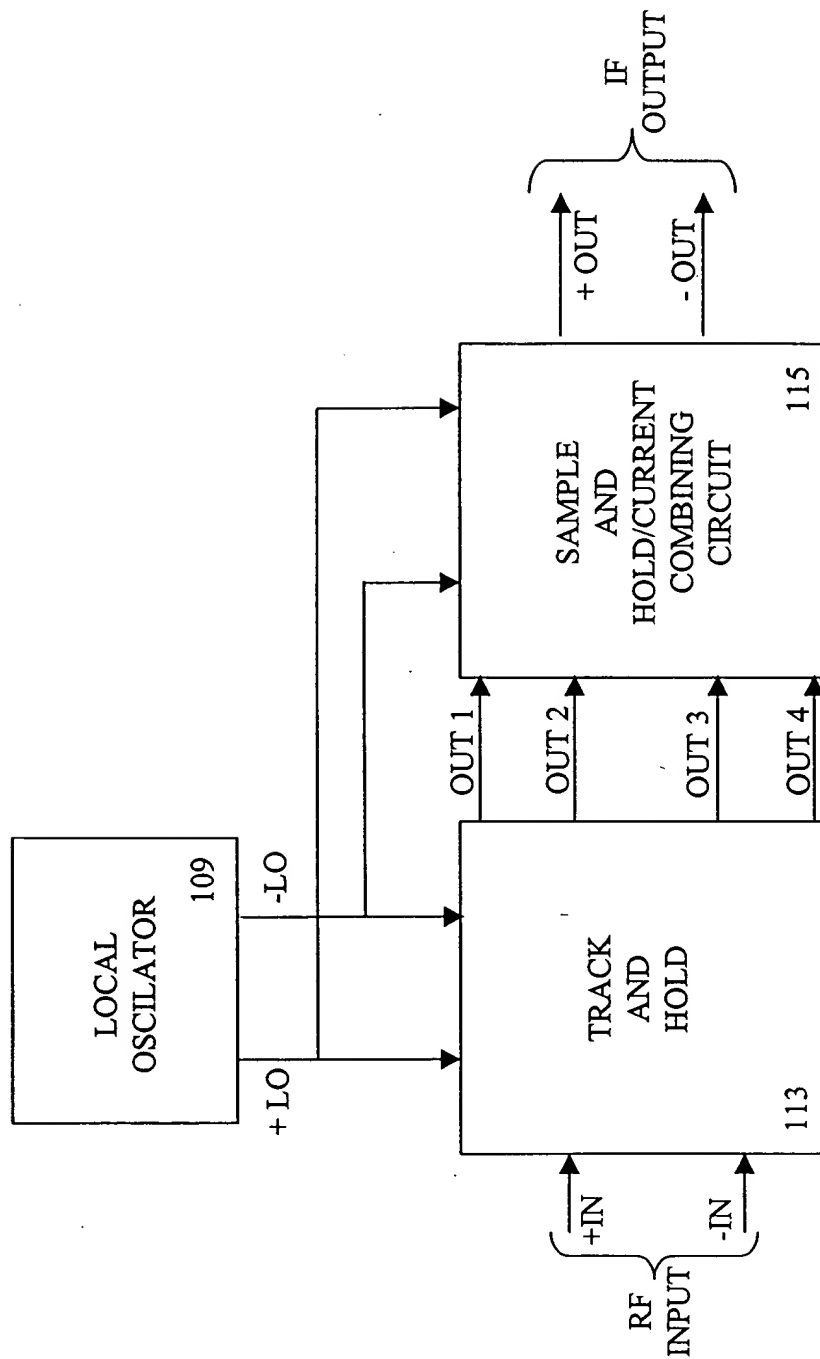


FIG. 30k



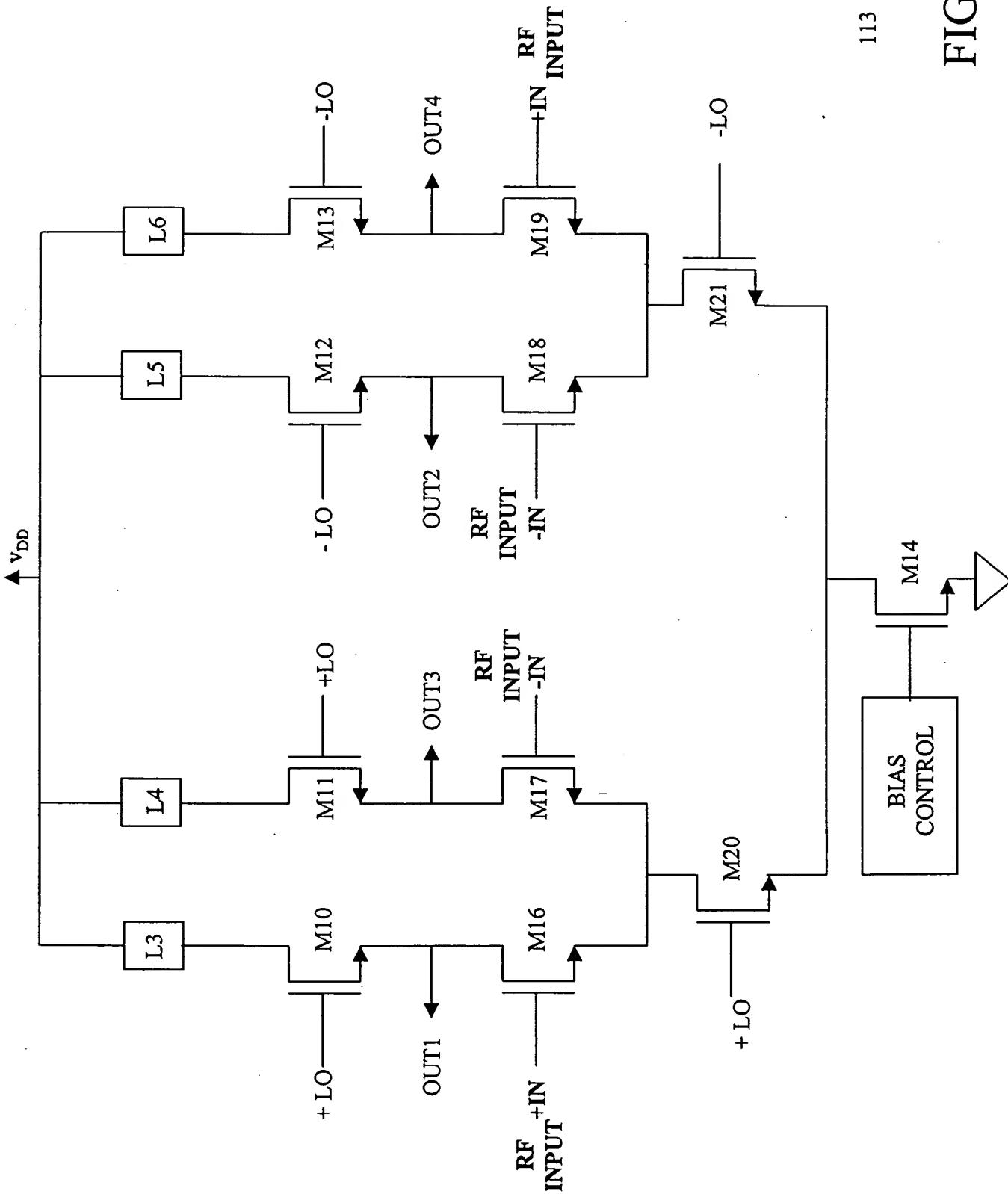


FIG. 30.m



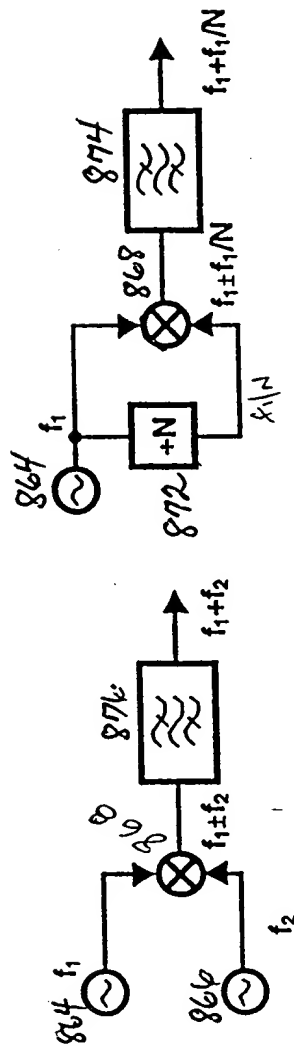


FIG. 31(a)

FIG. 31(b)

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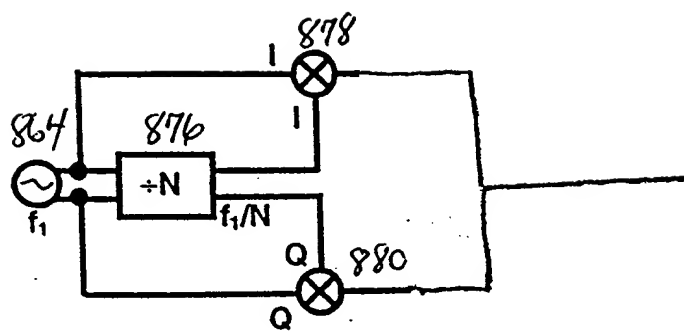


FIG. 32

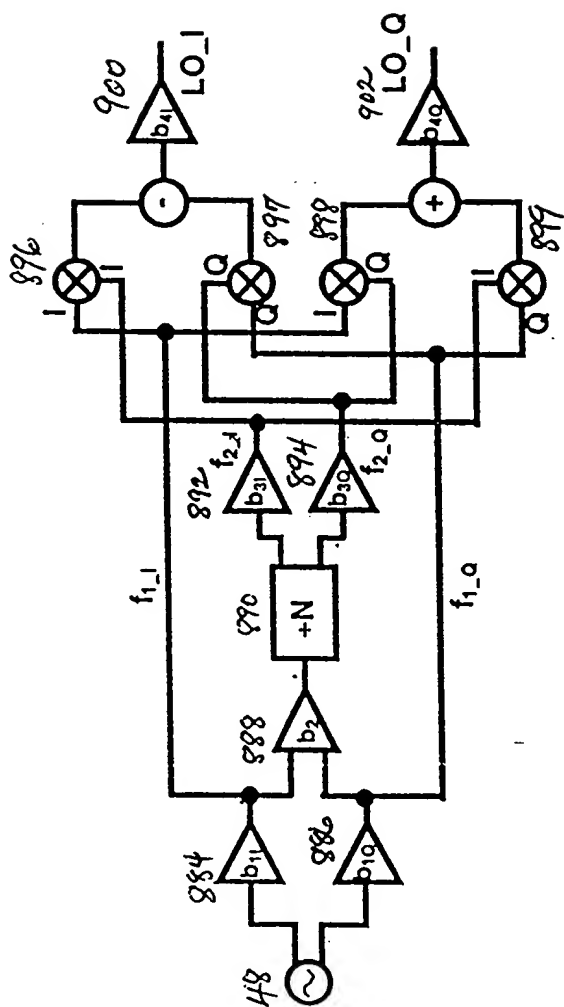


FIG. 33(a)



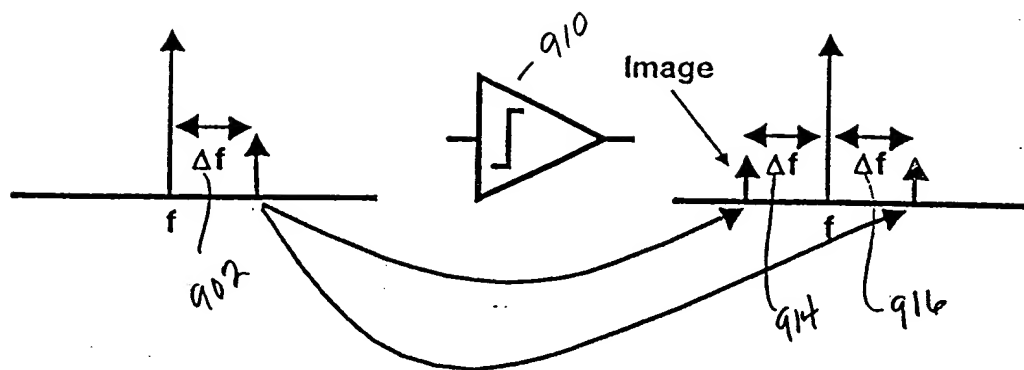


FIG. 33(b)

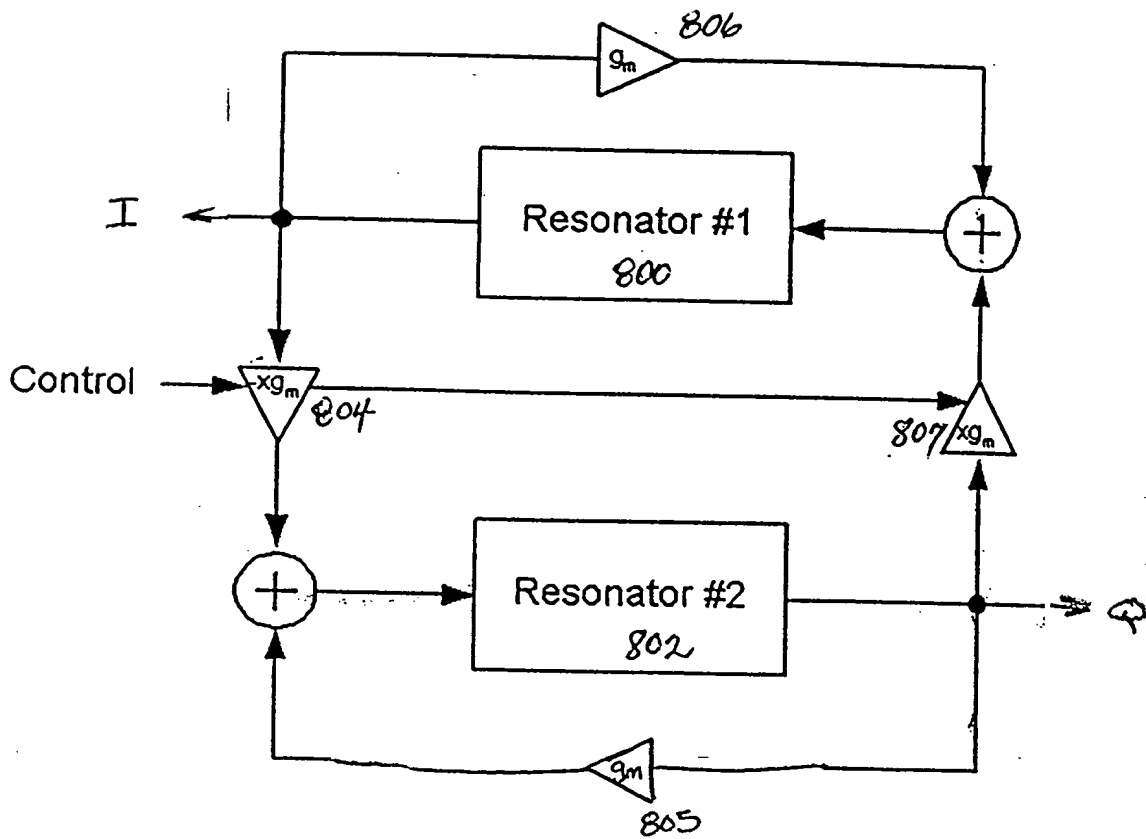


FIG. 34

The diagram illustrates a two-stage electronic circuit, likely a differential amplifier or a signal processing unit. The top stage consists of a bridge network with resistors 826, 828, 818, and 820. A central resistor 810 is connected to the bridge's center point. The input is connected to the bridge through resistor 834, and the output is connected through resistor 836. The bottom stage is similar, with a bridge network of resistors 830, 832, 822, and 824, a central resistor 814, and input/output resistors 838 and 840. Both stages are connected to a common ground at the bottom.

FIG. 35

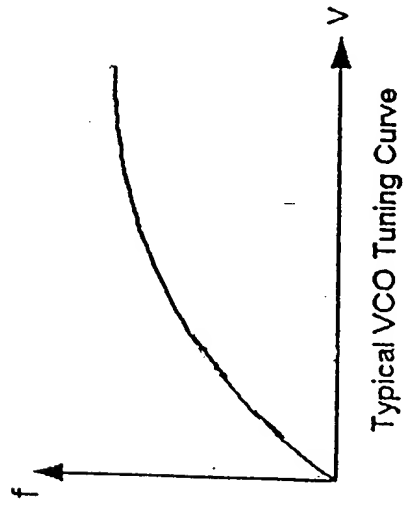


FIG. 36(a)

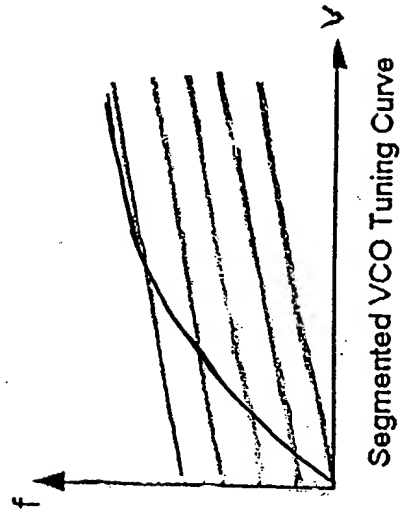


FIG. 36(b)

FIG. 37(a)

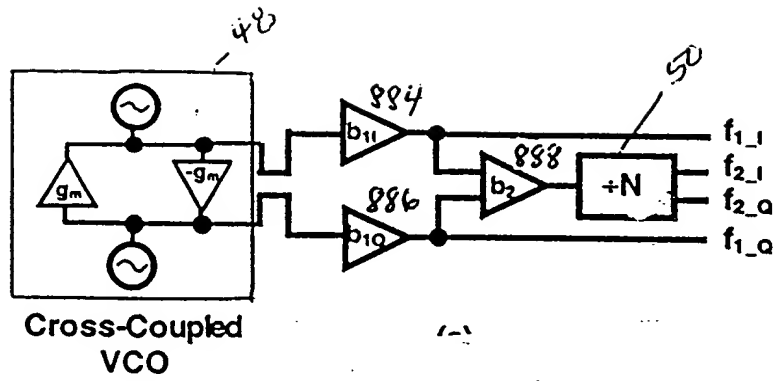
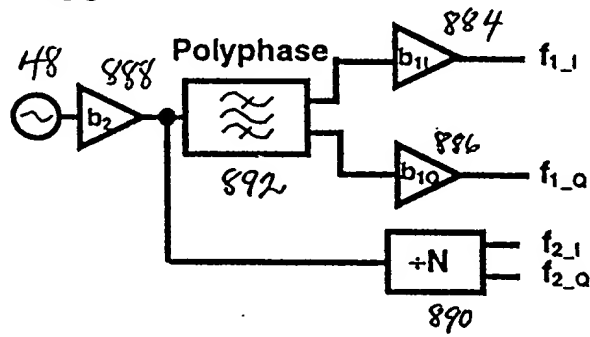


FIG. 37(b)



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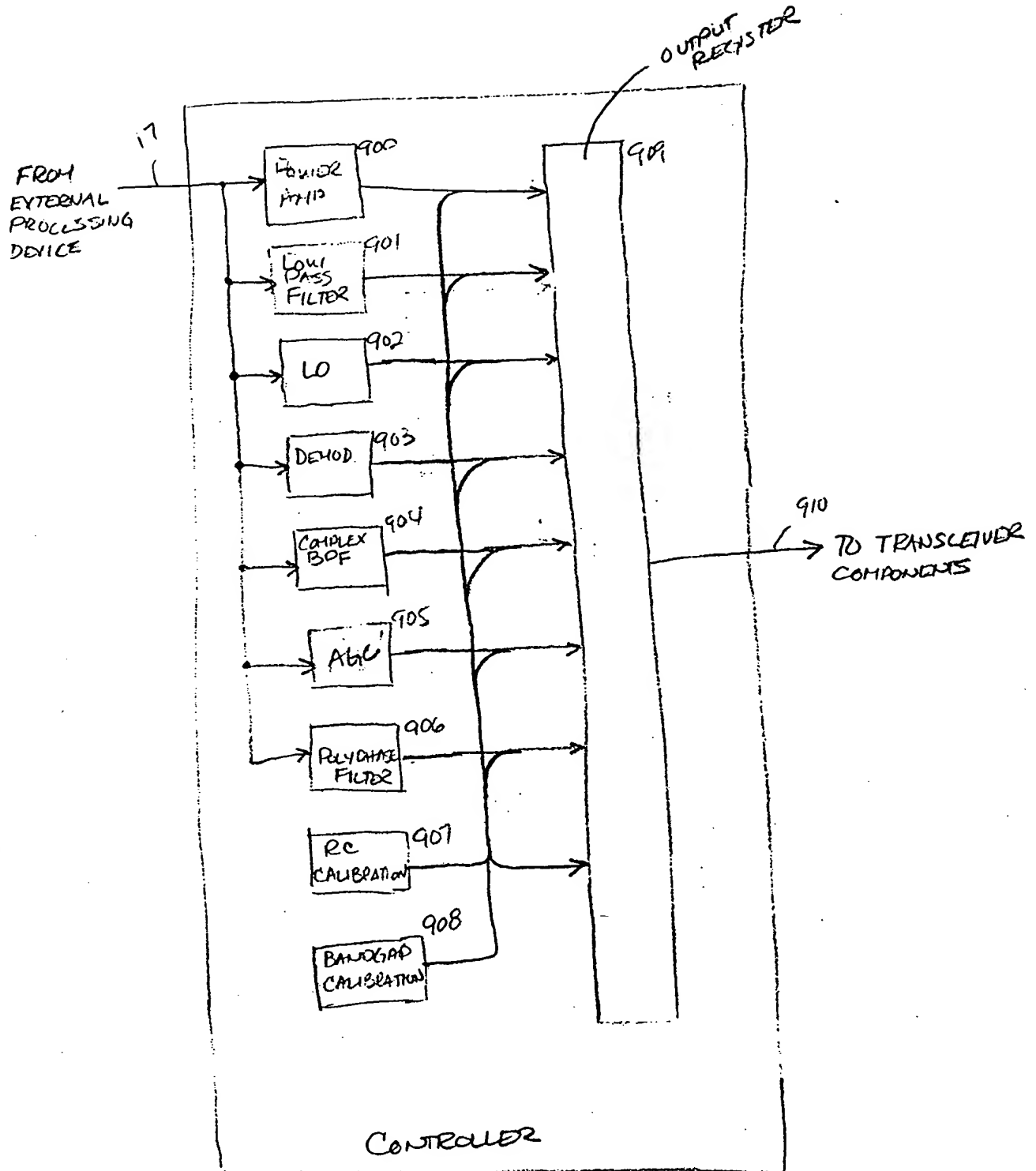


FIGURE 38

090909-011000

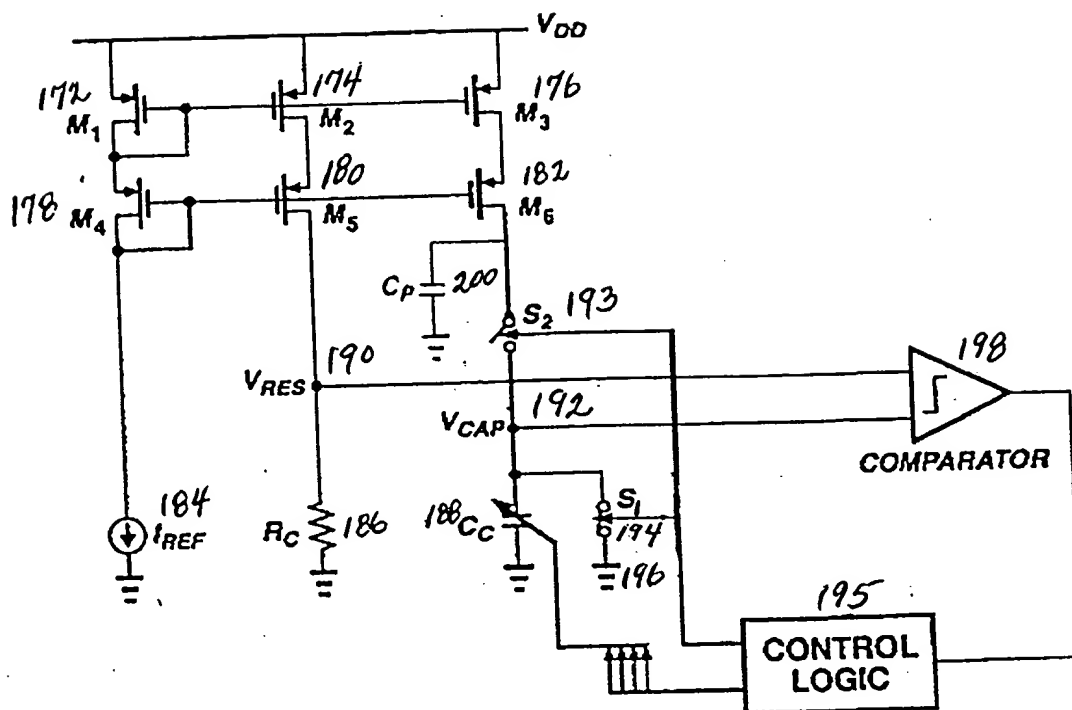


FIG. 39

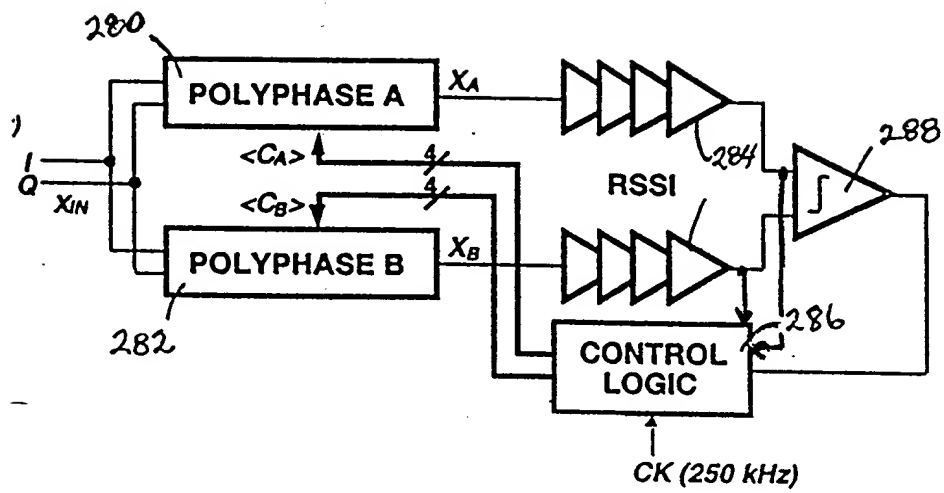


FIG. 40



098949 101200

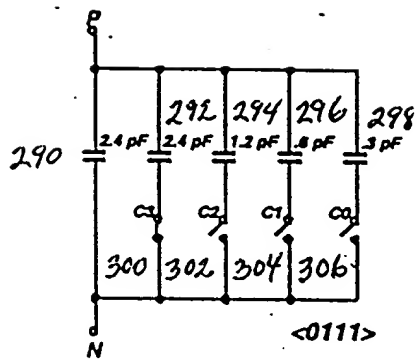


FIG. 41

002207" 25486950

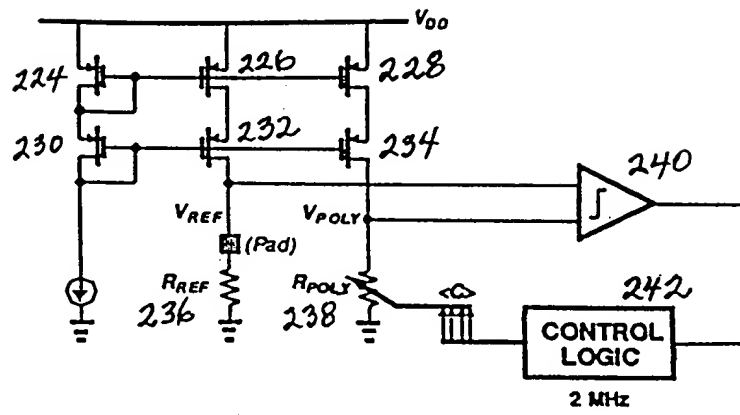


FIG. 42

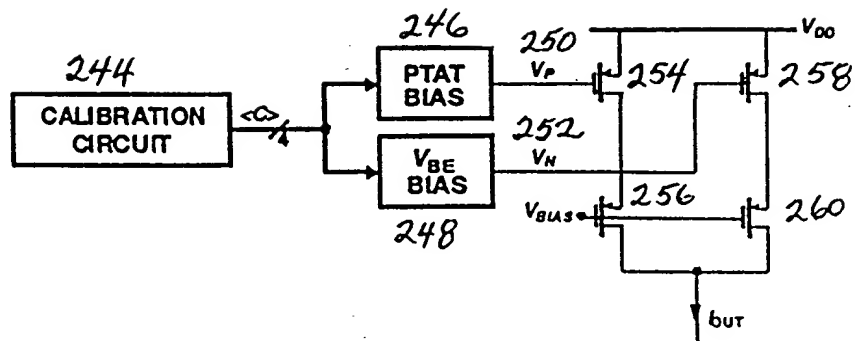


FIG. 43

FIG. 44

09698497-102700

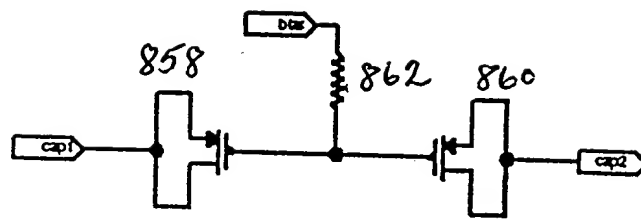


FIG. 45

002207" 25486960

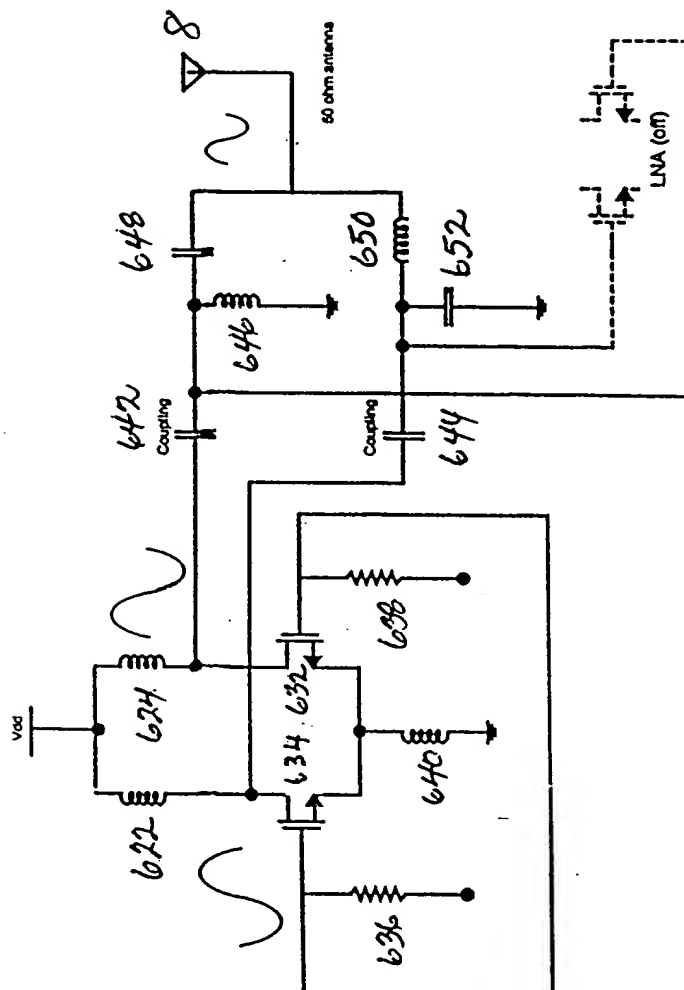


FIG. 46

09698497-102700

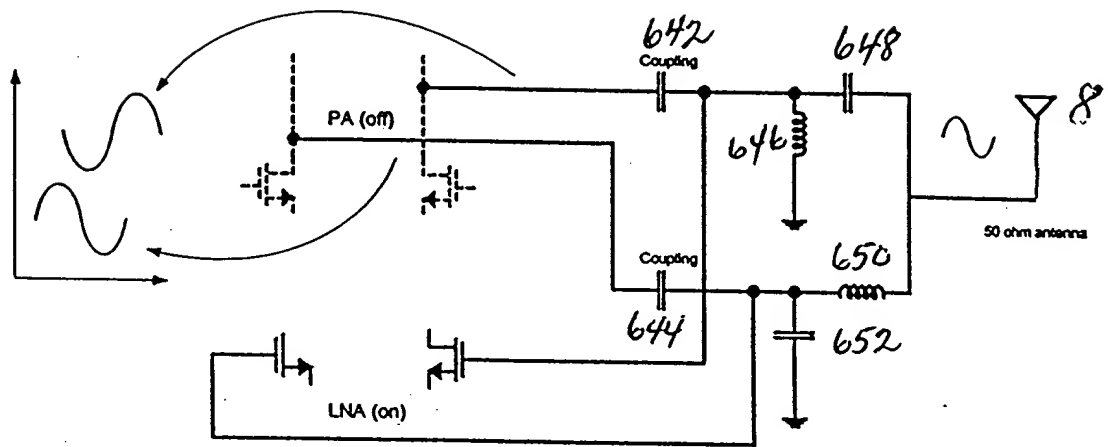


FIG. 47

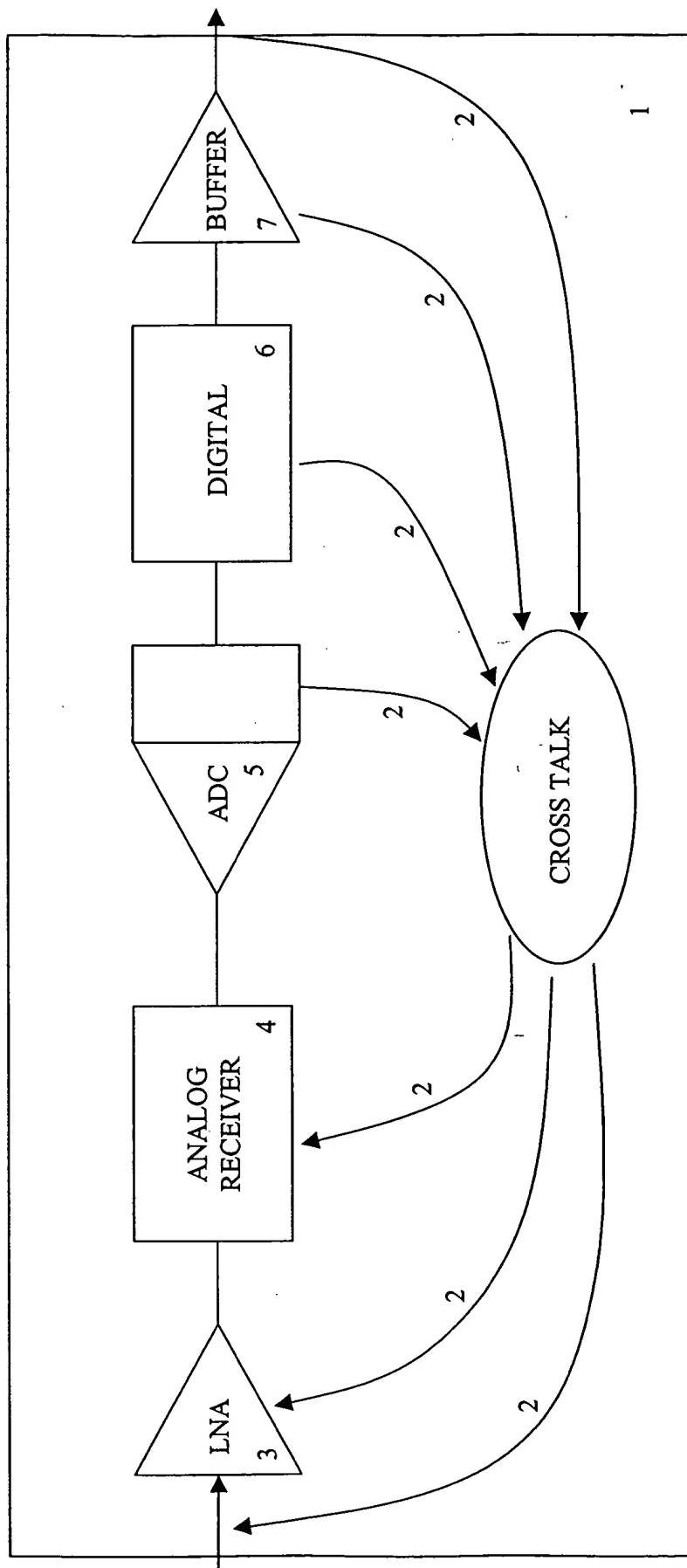


FIG. 48a



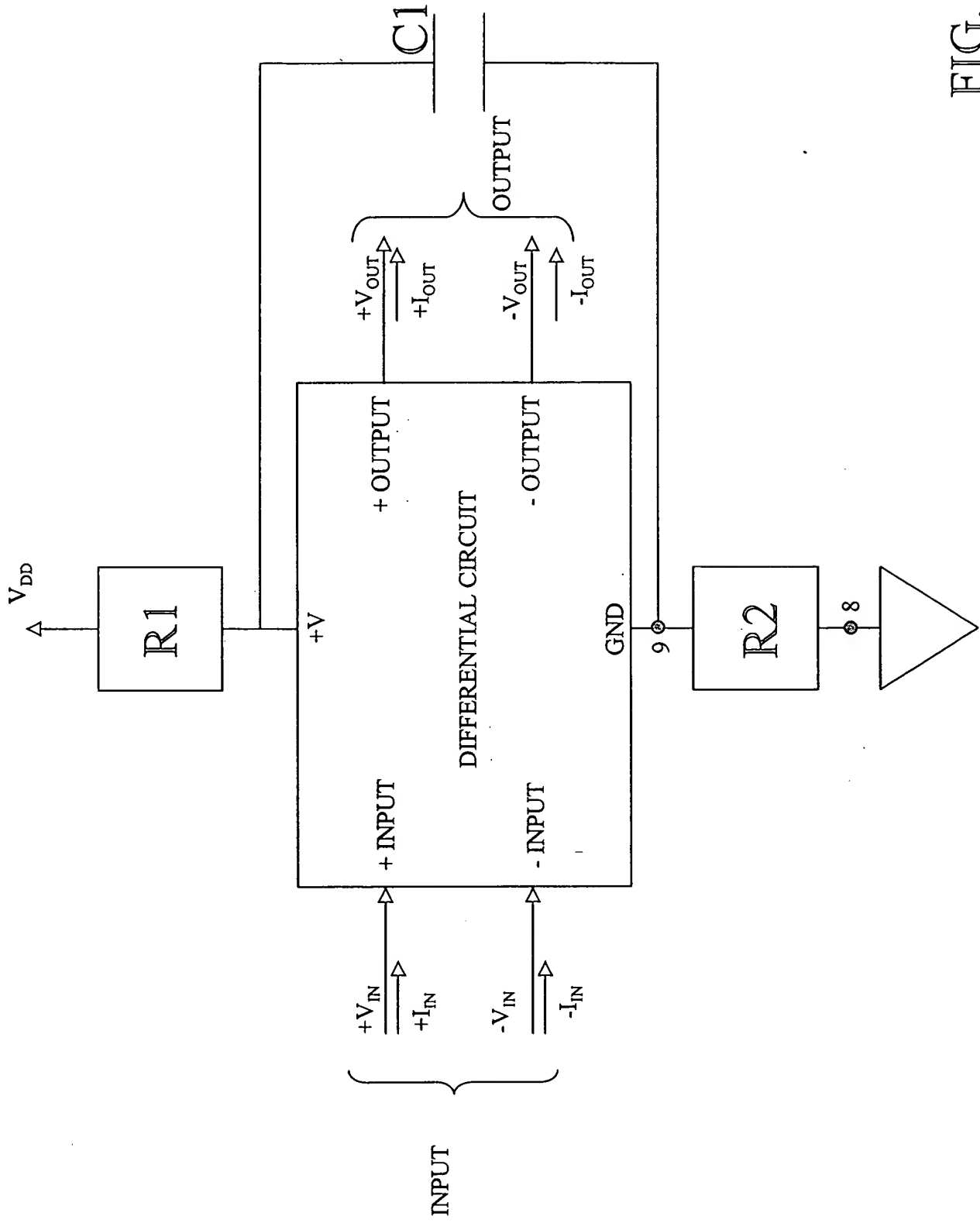


FIG. 406

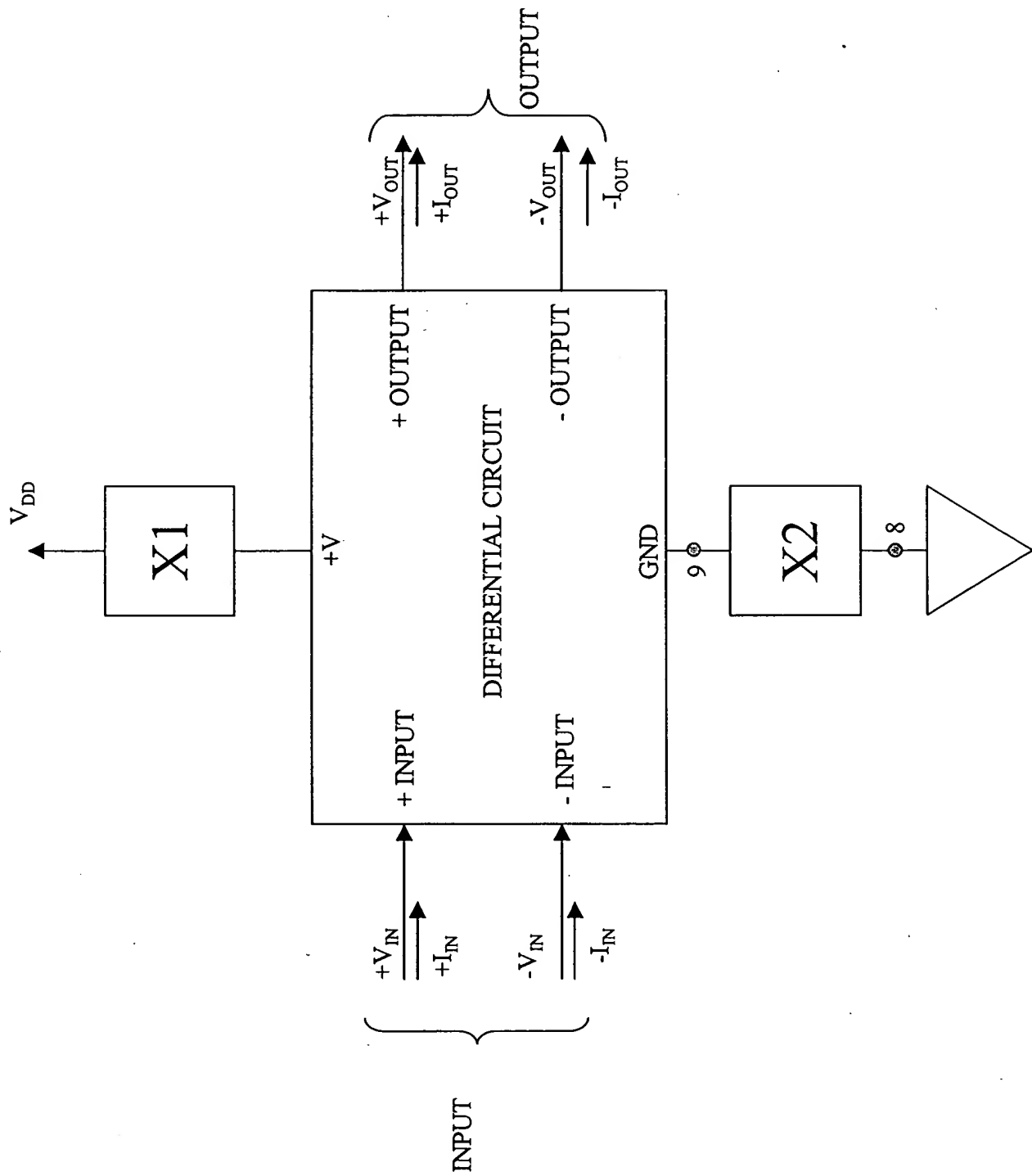


FIG. 48c

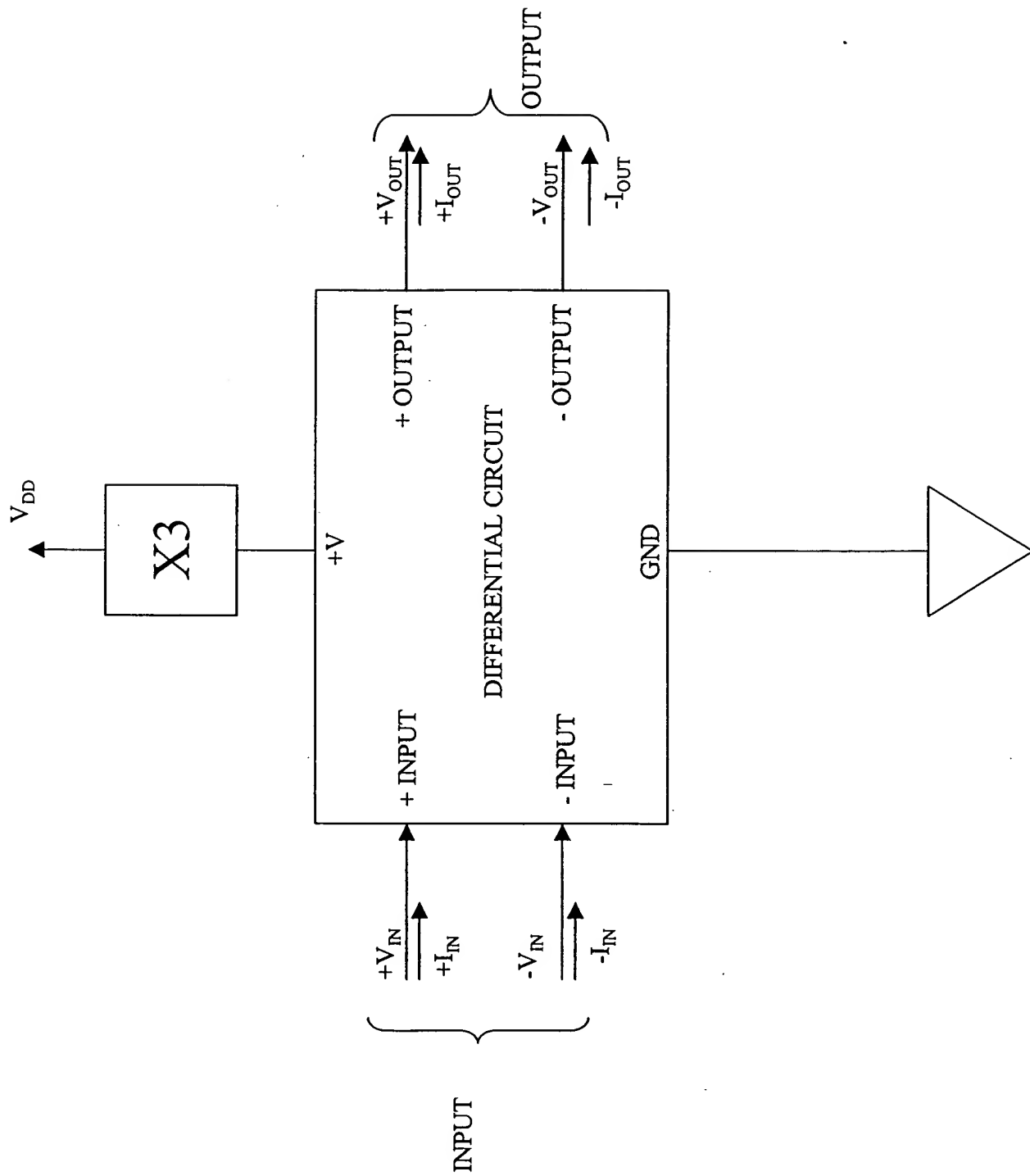


FIG. 48d

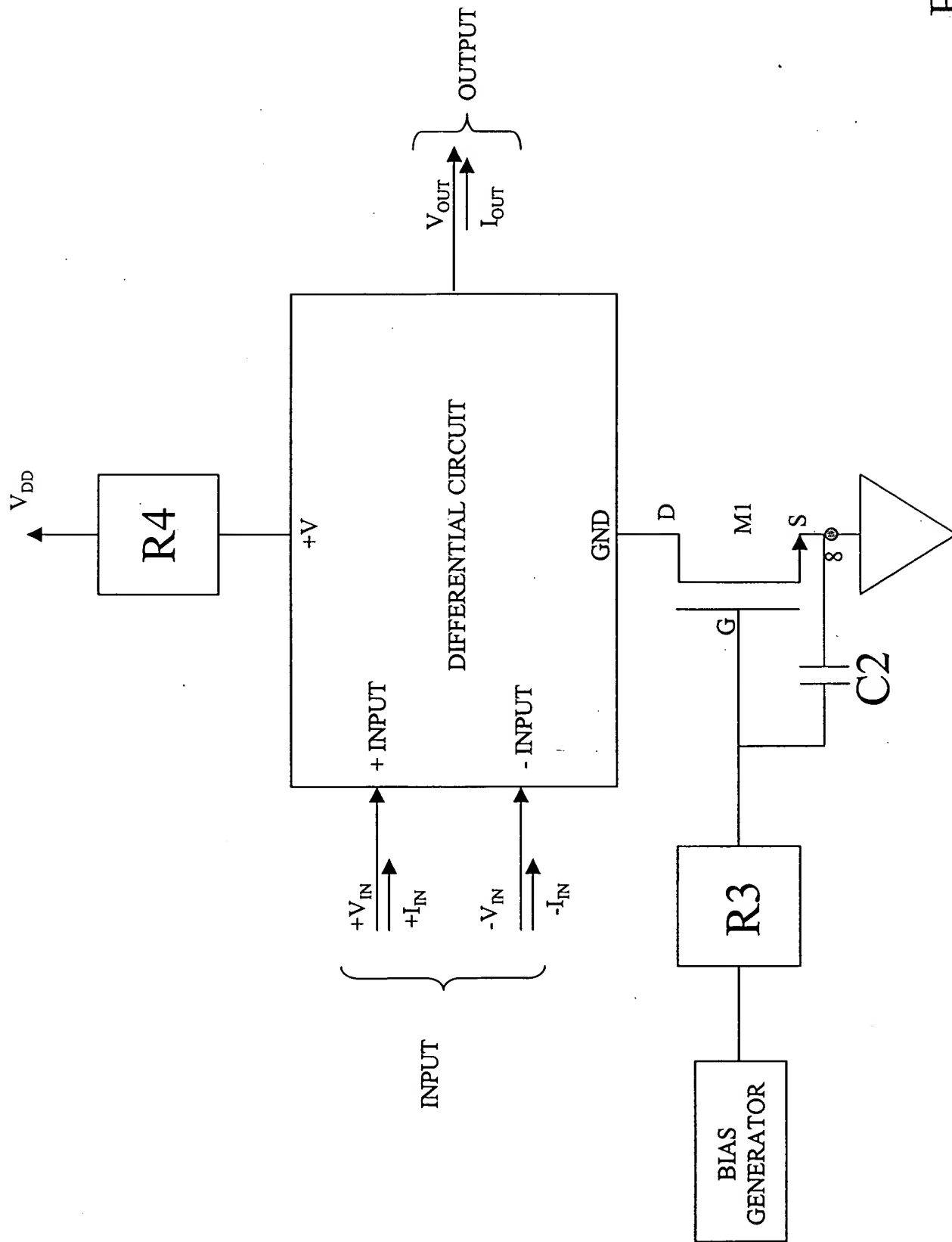


FIG. 48e

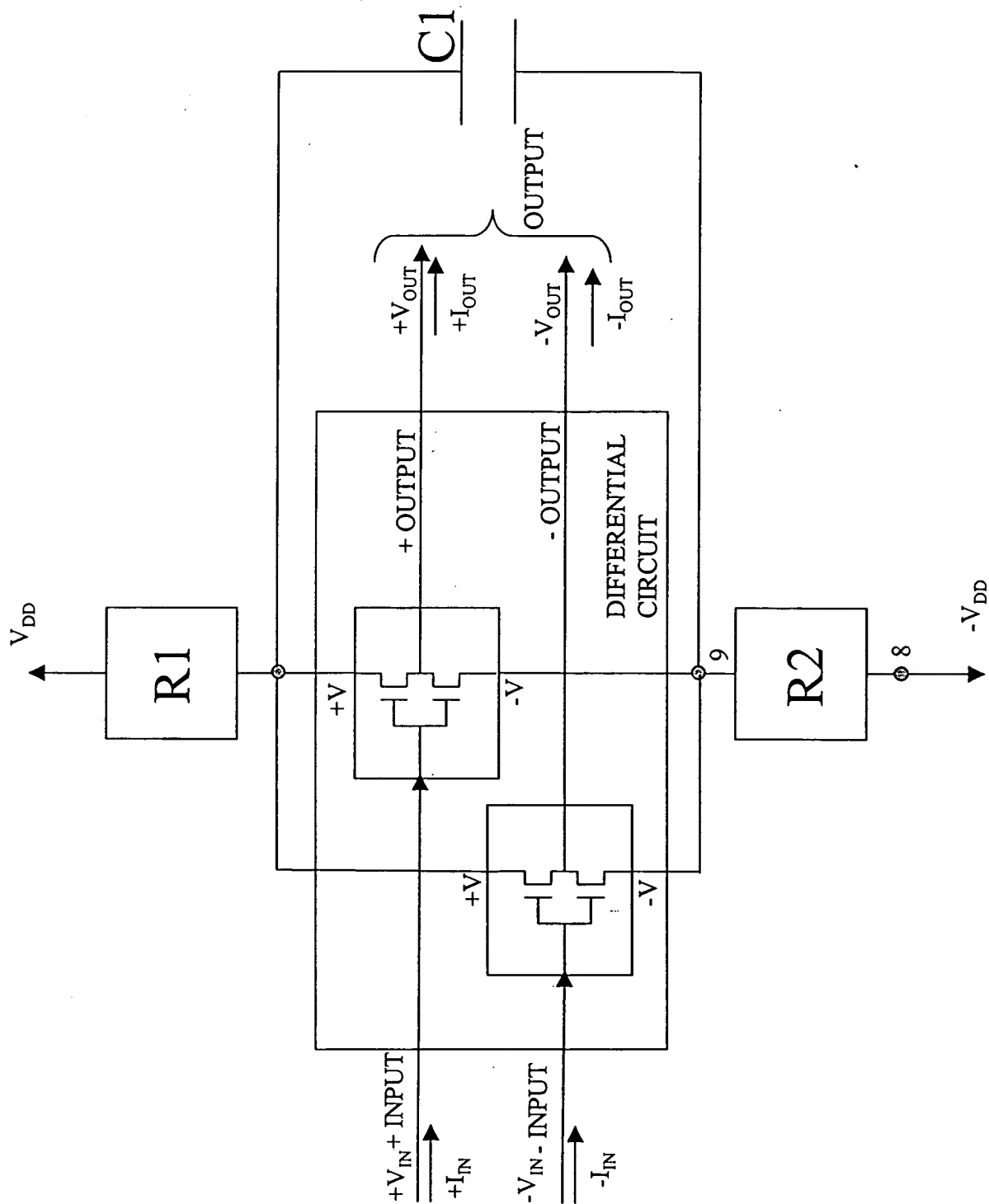


FIG. 48f